A High Performance Transistorised Power Source

For

MIG Welding

by

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November 1986
Memorandum

List of principal symbols

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MEMORANDUM

The accompanying thesis is based on work carried out by the author as a part-time postgraduate student in the Engineering Department of the University of Leicester between October 1980 and October 1986. The practical aspects of the work presented were carried out by the author whilst in the employment of Automated Welding Products during the period October 1980 to October 1984.

All the work recorded in this thesis is original unless otherwise acknowledged in the text or by reference. None of the work has been submitted for another Degree at this University, or for the award of a Degree or Diploma of any other institution.

The main contributions the author claims to have made to the subject of advanced arc welding power supplies include the following:

1. A digital computer model of a high frequency, high current chopper circuit that includes the effects of stray inductances, device electrical characteristics and a variable load impedance

2. Optimisation of the switching characteristics of power transistors at high currents using active de-saturation of the devices at turn off

3. A current control system has been developed that uses a PWM strategy that varies dynamically between a fixed frequency, variable pulsewidth and variable frequency,
fixed pulsewidth to regulate the load current over a wide range of arc impedances (including shortcircuits)

4. The successful use of constant current characteristic power sources for Dip Transfer MIG welding

5. For Dip Transfer MIG welding, a relationship has been identified between arc current and wire feed rate; this was used to reduce the operator controls to a single variable parameter (wirefeed rate)

6. Arc instabilities, hitherto unreported, have been identified

7. A double loop control system has been developed that regulates arc current and arc voltage simultaneously - to produce a MIG power source with a constant energy output characteristic

A.C.D.R. Rodrigues
November 1986
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<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
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<tr>
<td>Cs</td>
<td>snubber capacitance</td>
<td>microfarads (uF)</td>
</tr>
<tr>
<td>Fo</td>
<td>chopper modulating frequency</td>
<td>Hertz (Hz)</td>
</tr>
<tr>
<td>Ib</td>
<td>Pulse background current</td>
<td>Amperes</td>
</tr>
<tr>
<td>Ip</td>
<td>Pulse peak current</td>
<td>Amperes</td>
</tr>
<tr>
<td>Im</td>
<td>average welding current</td>
<td>Amperes</td>
</tr>
<tr>
<td>Iref</td>
<td>reference/demanded current</td>
<td>Amperes</td>
</tr>
<tr>
<td>IL</td>
<td>load/arc current</td>
<td>Amperes</td>
</tr>
<tr>
<td>iT</td>
<td>transistor collector current</td>
<td>Amperes</td>
</tr>
<tr>
<td>IF</td>
<td>flywheel diode current</td>
<td>Amperes</td>
</tr>
<tr>
<td>IS</td>
<td>snubber current</td>
<td>Amperes</td>
</tr>
<tr>
<td>L</td>
<td>inductance</td>
<td>microhenries (uH)</td>
</tr>
<tr>
<td>P</td>
<td>Power dissipation</td>
<td>Watts (W)</td>
</tr>
<tr>
<td>Qrr</td>
<td>diode recovered charge</td>
<td>microcoulombs (uC)</td>
</tr>
<tr>
<td>R</td>
<td>Resistance</td>
<td>ohms (Ω)</td>
</tr>
<tr>
<td>Tf</td>
<td>transistor current fall time</td>
<td>microseconds (us)</td>
</tr>
<tr>
<td>Tr</td>
<td>transistor turn-on time</td>
<td>us</td>
</tr>
<tr>
<td>Ts</td>
<td>transistor storage time</td>
<td>us</td>
</tr>
<tr>
<td>Ton</td>
<td>transistor conduction time</td>
<td>us</td>
</tr>
<tr>
<td>Toff</td>
<td>transistor OFF time</td>
<td>us</td>
</tr>
<tr>
<td>tR</td>
<td>pulsed load current rise time</td>
<td>milliseconds (ms)</td>
</tr>
<tr>
<td>tF</td>
<td>pulsed load current fall time</td>
<td>ms</td>
</tr>
<tr>
<td>Tb</td>
<td>pulsed current background time</td>
<td>ms</td>
</tr>
<tr>
<td>Tp</td>
<td>pulsed current peak time</td>
<td>ms</td>
</tr>
<tr>
<td>V</td>
<td>Voltage</td>
<td>volts (V)</td>
</tr>
<tr>
<td>Uce</td>
<td>collector-emitter voltage</td>
<td>volts</td>
</tr>
<tr>
<td>Vi</td>
<td>d.c. supply voltage</td>
<td>volts</td>
</tr>
<tr>
<td>Vm</td>
<td>average arc voltage</td>
<td>volts</td>
</tr>
<tr>
<td>X</td>
<td>reactance</td>
<td>ohms</td>
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List of MIG welding terminology

<table>
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<tr>
<th>Term</th>
<th>Description</th>
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<td>MIG</td>
<td>Metal Inert Gas process where one of the electrodes is the workpiece, the other the wire that is burnt off.</td>
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<tr>
<td>Dip Transfer</td>
<td>a MIG process where the filler wire shortcircuits repetitively to the workpiece</td>
</tr>
<tr>
<td>Filler Wire</td>
<td>mild/stainless/aluminium wire that is deposited on the workpiece to form the weld</td>
</tr>
<tr>
<td>Shielding Gas</td>
<td>Argon or Helium gas that is used to protect the hot weldpool from oxidation and contamination</td>
</tr>
<tr>
<td>Weldpool</td>
<td>molten metal formed on the workpiece as a result of arc heating</td>
</tr>
<tr>
<td>Burnoff</td>
<td>wire heating and melting process</td>
</tr>
<tr>
<td>Spatter</td>
<td>stray metal droplets deposited on the workpiece</td>
</tr>
<tr>
<td>Metal Transfer</td>
<td>mechanism involved in the detachment of metal droplets from the wire</td>
</tr>
<tr>
<td>Synergic</td>
<td>a generalised form of the pulsed current transfer process</td>
</tr>
<tr>
<td>Transition current</td>
<td>current level at which the filler wire burns off continuously to form an open (spray) arc</td>
</tr>
<tr>
<td>Standoff</td>
<td>distance between torch nozzle orifice and workpiece</td>
</tr>
<tr>
<td>Stickout</td>
<td>length of filler wire between the arc anode and the electrode contact tip</td>
</tr>
<tr>
<td>Contact tip</td>
<td>copper piece through which the wire is fed and makes electrical contact</td>
</tr>
<tr>
<td>Weld Bead Profile</td>
<td>shape of weld deposited</td>
</tr>
<tr>
<td>Coldlapping</td>
<td>where the hot metal droplets are deposited into a weldpool that is too cold to form a homogeneous bond</td>
</tr>
<tr>
<td>Workpiece/plate</td>
<td>materials being welded together (at electrode -ve potential )</td>
</tr>
<tr>
<td>Reinforcement Area</td>
<td>area of weldment above the surface of the weld</td>
</tr>
<tr>
<td>Fusion area</td>
<td>area of weld under surface</td>
</tr>
</tbody>
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ABSTRACT

This research concerns an investigation into the application of Power Electronics to high performance power sources for precise and efficient control of the pulsed-current metal-inert gas (PCM) welding processes. The physical processes of the welding arc are reviewed and the characteristics of a number of power sources are considered prior to preparing the operational specification for the PCM power source. From a number of possibilities the high frequency switching regulator operating in the secondary side of the power transformer was selected for detailed study.

The power source was based on the use of state-of-the-art power transistors operating in a switching mode to minimise losses and to give a fast response for good welding performance. The basic operating frequency was chosen to be at the very limit of the audio range. The dynamic behaviour of the transistors and associated protection networks is critical and failure to meet all the operating limits of the transistor can be costly. To assist with the thorough understanding of the circuit behaviour and to predict the transistor switching waveforms a digital computer model was developed. This gave good correlation with experimental results observed with the completed power source.

Tests were carried out with the welding power source and showed that there was no discernable difference in the weld quality when compared with those produced by the more expensive series linear regulator power source. As a direct result of the study a new range of power sources meeting exacting standards have been made available to the welding industry.
1. THE ARC WELDING PROCESS

1.1 Introduction

Fusion arc welding is the most common method used for the joining of ferrous and non-ferrous metals. A number of diverse arc processes are in present use - covered electrode, submerged arc, resistance welding, gas shielded arc welding etc and these account for over 80% of metal tonnage arc welded. Arc welding is however one of the least productive methods of joining metals (Figure 1.0) and compares very unfavourably, for example, against the electron beam and laser welding processes. Despite its limitations, the arc welding process has the advantages of low capital and running cost, mobility of the equipment and capability of use in manual and mechanised operations.

The Manual Metal Arc ("stick") process is widely used for general metal fabrication whereas the Metal Inert Gas (MIG) and Tungsten Inert Gas (TIG) arc processes are associated with medium and high quality fabrication. The MIG process is prone to producing weld defects (due to the lack of fusion between the metals being welded), metal spatter and poor weld appearance - the result of the use of crude power control methods. Recent developments in the MIG process and equipment have virtually restored MIG welding as a viable alternative to other higher quality arc processes. This has been achieved with the use of more
1. Least thickness dimension in butt welding for various joint configurations.

2. Comparison of welding processes by thickness range for single pass unbacked butt joints in mild steel.

3. Joining rate as the product of total length and depth of weld accomplished in unit time.

4. Comparison of welding processes by joining rate for mild steel.

FIGURE 1.0
sophisticated power sources, giving precise control of arc current and voltage, predetermined metal transfer characteristics and controllable heat input to the weld joint. The choice of consumables (gas, filler wire) is limited to those which are commercially available. In order to increase productivity and weld quality, the energy consumed by the arc needs to be more closely regulated. Furthermore, energy transfer from the power source to the weldpool needs to take place within an electrically stable arc (continuous ionisation of the shielding gas).

By examining the properties of the welding arc for different MIG processes, several authors have propounded power source characteristics that are required for producing:

a) high quality MIG welds in a stable arc environment
b) controlled metal and heat transfer through the arc
c) high metal deposition rates

The development of the Synergic Pulsed MIG Process at the Welding Institute (U.K.) in the early 1970's was carried out using transistorised Series Linear (CLASS A) Regulator (SLR) types of power sources whose output could be programmed electronically. The regulator consisted of up to 500 (2.5 Ampere) transistors connected in parallel to produce 500 Amperes of weld current from a 60-100V d.c. supply. The transistors have to absorb the difference between the power drawn from the supply (> 30 KW) and that consumed by the arc
as heat and light energy (5-25KW). This was accomplished by dissipating the power in a large number of water cooled transistors, making the manufacture of SLR types of power sources labour intensive and expensive.

SLR power sources are used for fundamental research into the welding process and for high quality welding of aerospace, nuclear and defence components. More recent research has shown that both metal transfer and weld properties are strongly (almost exclusively) dependent on weld current and hence the accuracy and repeatability of the required current is a prerequisite for high quality MIG welding. This has led to the recent introduction of constant current characteristic power sources for MIG welding, whereas conventional sets employ the constant voltage characteristic.

One of the drawbacks of current controlled MIG is the lack of arc length control which in the extreme cases could lead to arc instability and arc extinction. A method for controlling the arc length needs to be developed to alleviate these problems.

SLR power sources cost up to £30/Ampere restricting them to high quality metal fabrication industries. A power source needs to be developed which has SLR specifications but at a lower cost so that the benefits of Pulsed Current MIG welding, for example, could be made available to the medium and general fabrication
industries.

Conventional designs of welding power sources are based on thyristor and magnetic amplifier technology and do not have the bandwidth or accuracy of the SLR. By operating power transistors in a switching rather than linear mode of operation, device losses are reduced significantly. The earliest reported chopper welding power source was for TIG welding. Output current was limited to 100A by difficulties in device and circuit operation. The output waveforms of switched regulator types of power sources however, approach that of SLR's and hence could form the base technology for the development of a high performance low cost power source.

In the early 1980's, chopper based MIG power sources were introduced to the market. These operated at low modulating frequencies (< 5kHz). The welding performance of these sets was adequate and at costs approaching £10/Ampere. Their environmental characteristics (acoustic noise and fume emissions from the arc) and limited dynamic response are the main disadvantages of these sets. A higher modulating frequency, preferably above the audible threshold (15kHz) is required. Two basic circuit topologies, fundamentally different, need to be considered. The first is a secondary switched, high frequency (> 15kHz) chopper operating off a low d.c. voltage supply (< 100V).
The other is the primary inverter which operates off rectified three phase supplies (600V d.c.) to produce inversion to a.c. at a high frequency (as in Switched Mode Power Supplies).

By drawing parallels with the power supply industries, the primary switched mode power supply, despite all its advantages of size and weight, is still relatively expensive due to circuit complexity and the use of state of the art components. Furthermore, the servicing and maintenance of equipment in the field would require considerable investment by the customer in personnel training in the troubleshooting of high voltage circuitry. The low voltage chopper design, on the other hand, was viewed as a natural extension in performance of conventional welding set designs and hence more acceptable to the market.

A 500A MIG Power Source based on the high frequency transistor chopper was therefore selected for this research work. The project involved the design and development of a chopper power module which was used to produce an advanced MIG Power Source for Pulsed Current and Controlled Dip Transfer MIG welding. A computer model was developed to optimise the ratings of all the power components and predict the performance of the power source under load conditions.
2. THE METAL INERT GAS (MIG) WELDING PROCESS

2.1 Arc Welding Requirements

Welding is a process employed for joining two or more sections of materials across their common interfaces. The basic requirements for a fusion arc weld are:

a) a heat source for melting the materials at their common points of contact and their immediate surroundings

b) a shielding medium to protect the molten weld area from atmospheric contamination/oxidation

c) a consumable metal to fill up the weld preparation

The above welding arc requirements need to be accompanied by good metallurgical properties to the welded joint.

2.2 Review of the MIG Process

The Metal Inert Gas (commonly referred to as MIG/MAG) process was developed in the 1940's for the welding of aluminium alloys. Fusion of the joint is produced by the heat from an electric arc struck between a continuously fed filler metal (welding wire) and the workpiece (comprising the materials to be joined). Arc shielding is provided from a source of inert/active gas, usually a mixture of Argon/Helium/Carbon dioxide.

The basic features of the equipment and process are shown in Figure 2.1a,b.

The MIG Process is further defined by the method of
EQUIPMENT ARRANGEMENT FOR THE MIG PROCESS

FIGURE 2.1a

SCHEMATIC OF MIG PROCESS ARC

FIGURE 2.1b
metal transfer - Spray, Dip, Globular and Drop. The Spray and Dip Transfer modes are the most common. In all of the above processes, the following process properties are required:

a) controlled heating of the workpiece and tip of the filler wire

b) the volume and the rate of detachment of the metal droplets need to be defined and maintained

c) a preferred mode of metal transfer (Dip, Spray, Pulse) needs to be maintained continuously during a welding cycle

d) the detached metal droplet needs to be projected axially into the weldpool; (in Dip Transfer, the droplets are detached at the position of short circuiting and hence metal can be deposited accurately within the joint preparation; in Spray Transfer, the droplets are guided into the preparation by arc forces and this requires a stable and directional arc)
2.3 Theoretical Background to the MIG Processes

2.3.1 Arc Characteristics

The MIG arc consists of three sections (Figure 2.2a)

a) the cathode and cathode drop region

b) the arc column

c) the anode and anode drop region

The arc voltage is the sum of the voltage drops of each of these regions. A typical MIG arc voltage-ampere characteristic is shown in Figure 2.2b. It exhibits a negative resistance region at low arc currents and a positive resistance region at higher currents. The general shape of this characteristic is maintained for changes in shielding gas, filler wire composition and torch-workpiece separation.

The arc characteristic can be expressed as follows:

\[ V_m = A + B.I_m + C/I_m \]  

where \( V_m \) = arc voltage

\( I_m \) = arc current

A, B, C are constants that are gas and wire composition dependent

The minimum arc voltage for a stable arc condition is 18-20V for argon based gases and 22-24V for helium based gases. The interaction between the arc and power source characteristics is shown in Figure 2.3. Stable operating points in the negative resistance regions of the arc curve are only possible if the power source can maintain the demanded arc voltage under transient and steady state conditions.
Schematic representation of the three different regions of the electric arc

![Diagram showing cathode drop region, arc column, and anode drop region.](image)

**FIGURE 2.2a**

Arc characteristic with different arc lengths

![Graph showing voltage (V) vs. current (A) for different arc lengths.](image)

**FIGURE 2.2b**
Interaction between the arc load and power source characteristic

FIGURE 2.3
2.3.2 Heating and Melting Mechanisms

The electrical energy supplied by the power source is the only input of energy into the welding arc. The distribution of this energy within the MIG welding arc has been and still is the subject of a number of theories, of which, one by Wasnik has proved to be the most acceptable to researchers.

The electrical energy is converted into heat, light and radiation within the arc column and at the anode (wire tip) and cathode (workpiece) regions of the arc. All of this energy is ultimately lost to the environment surrounding the arc. Some of this energy is utilised productively to heat and melt the filler wire and to create and maintain the weldpool at the required temperature and fluidity. The energy balance is given by:

\[ \text{Ha} + \text{Hc} + \text{Hj} = \text{Hh} + \text{Hm} + \text{Hw} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2) \]

where

- \text{Ha} = \text{arc anode heating}
- \text{Hc} = \text{arc cathode heating}
- \text{Hj} = \text{Joule heating of wire tip}
- \text{Hh} = \text{energy required to heat the wire tip to its melting point}
- \text{Hm} = \text{energy required to melt the wire}
- \text{Hw} = \text{energy required to form the weldpool}

2.3.3 Arc Heating (reference Figure 2.2a)

a) Anode heating: The energy (Ha) gained from the arc at the anode is due to
i) the energy gained by electrons accelerating through the anode drop region ($V_a.I_m$)

ii) thermionic energy released at the anode due to electron recombination

iii) thermal energy of the hot electrons

These are collectively given by:

$$H_m = I_m \times \text{constant}$$

where the constant is estimated at approximately $6.3V^{14}$ and $I_m = \text{arc current}$. This shows that anode arc heating is a function of arc current ($I_m$) only.

b) Cathode heating: The energy supplied to the cathode is that acquired by the gas and metal vapour ions accelerating through the cathode drop region, and is given by:

$$H_c = I_m \cdot V_c$$

which again is a function of arc current.

### 2.3.4 Joule Heating

The filler wire consists of a molten tip and a solid heated section. Wasnik concluded that most of the heat required to heat the wire tip to its melting point was due to the resistive heating of the wire tip

$$H_j = I_m \times R$$

where $R = \text{Resistance of wire tip (length L)}$

For mild steel, 1.2mm diameter wire, Resistance $R$ is estimated at between 15 and 35 milliohms .......(6)

(for $100 < I_m < 250$ amps and $25 < L < 55$ mm)
2.3.5 Heat Consumption

The total heat generated is consumed in:

i) wire heating and melting to form a molten droplet

ii) superheating of the molten droplet as it travels across the arc column

iii) vaporisation of some of the liquid metal

iv) workpiece melting to produce the weldpool and maintain its fluidity

v) radiation from the anode spots, dissociation of the shielding gas molecules, heat conduction through the wire and shielding gas to the surroundings etc.

The efficiency of the spray MIG process has been measured at between 45% - 65%. This assumes that all the metal melted from the wire is transferred to the weldpool. The efficiency is even lower if loss of metal due to spatter is considered.

2.4 Metal Transfer Mechanisms

The molten metal formed at the tip of the filler wire detaches and is transferred through the arc column and into the weldpool under the influence of a number of forces (Figure 2.4).

2.4.1 Electromagnetic Forces (Lorentz Force).

The electromagnetic force (Fm) is created by the interaction between the arc current and its own
magnetic field. The magnitude of this force is given by

\[ F_m = \frac{U_0 \cdot I_m^2}{4.\pi \cdot x} \]  \hspace{1cm} \ldots \ldots \ldots (7)

where \( x \) = diameter of conductor
\( I_m \) = arc current
\( U_0 \) = constant

The effect of the radial forces is the cause of the "necking" of the molten length of wire at the solid-liquid boundary - Figure 2.4. This detachment mechanism is dominant in the spray transfer process.

2.4.2 Surface Tension Forces

The Surface Tension Forces act to hold the molten droplet in a spherical form and works against the forces of detachment.

\[ F_s = 2.\rho \cdot x. \]  \hspace{1cm} \ldots \ldots \ldots (8)

where \( x \) = droplet radius
\( \rho \) = surface tension force

2.4.3 Gravity Forces

The Gravitational forces aid droplet detachment in downhand welding and oppose it in vertical and overhead welding positions.

\[ F_g = mg \]  \hspace{1cm} \ldots \ldots \ldots (9)

where \( g \) = gravitational force
\( m \) = mass of droplet

2.4.4 Other Forces

Other forces that have a secondary role in metal detachment are due to gas drag (\( F_d \)) and arc repulsive mechanisms (\( F_r \)).
Forces acting on the electrode tip

**FIGURE 2.4**

**FIGURE 2.5**

Relationship between the wire melting rate and welding current for 1.2mm diameter mild steel wire (shielding gas, Ar + 5% CO₂)
2.5 Metal Transfer Modes

Much of the present day thinking about metal transfer stems from the work done by Cooksey and Milner. Metal detachment occurs in three clearly defined bands of current (Figure 2.5), the transfer modes (Figure 2.6) being primarily of globular, dip and spray types.

2.6 Process Description and Analysis

2.6.1 Dip Transfer

In the Dip Transfer process, the wirefeed rate and wire burnoff rate are chosen such that repetitive short circuiting occurs between the wire and weldpool. Metal is deposited into the weldpool during the shortcircuit period. The basic steps of the Dip Transfer process and associated waveforms are shown in Figure 2.7. The process demands a rapid increase in current during the short circuit period followed by a peak power surge at the instant of separation of the molten tip from the wire. The principal problem with the Dip process is the high level of metal spatter on the weldment caused by the explosive rupturing of the weldpool at the instant of shortcircuited.

The Dip process is also prone to "coldlapping" i.e. the deposition of metal into a weldpool that is not hot enough to ensure good bonding between the workpiece material and the wire metal deposited.

These problems can be alleviated by pre-programming
Description of the different MIG processes

In Free Flight transfer, a continuous arc is maintained between the electrode and the workpiece and the metal is transferred to the weld pool as droplets. In the dip mode, the arc is periodically extinguished.

**Spray Transfer**

This mode of transfer consists of a 'spray' of very small molten metal droplets which are projected towards the workpiece by electrical forces within the arc. This mode of transfer is particularly suited to positional welding with Aluminium and its alloys.

**Dip Transfer**

At currents above those which produce dip transfer but below the current level required for spray transfer, globular transfer occurs. The droplet size is large relative to the wire diameter and transfer is irregular. This mode of transfer occurs with steel wires at high currents in CO₂, but is generally regarded as unsuitable unless high spatter levels can be tolerated. The use of cored wires gives a controlled form of globular transfer which is acceptable.

**Globular Transfer**

In pulse transfer, the droplets are transferred by a high current which is periodically applied to the arc. Ideally, one drop is transferred with each pulse and the droplet size is regular. The operating frequencies are 50 to 100 droplets per second. A background current is maintained between pulses to sustain the arc but avoid metal transfer.

**Pulse Transfer**

The wire is fed at a rate which is just greater than the burn-off rate for the particular arc voltage being used, as a result the wire touches the weld pool and short circuits the power supply. The filler wire then acts as a fuse and when it ruptures a free burning arc is created. This phenomenon is repeated regularly up to 200 times every second. The net effect is a continuous welding condition with a low heat input and small weld pool.
Schematic diagram of the process of short circuiting metal transfer in MIG welding.

Diagrammatic representation of the short term fluctuation in the welding current waveform

FIGURE 2.7
the power source to achieve adequate heat input rather than rely on the skill of the operator in setting the power source controls.

**Improvements in fusion properties in Dip Transfer**

Total heat supplied to the workpiece is given by:

\[ P_w = P_m + I_m K_a \]

\[ ........ (10) \]

where \( P_m \) = energy of droplets (\( \propto \) wire feed rate)

\( K_a \) = arc length constant

This indicates that the heating of the workpiece can be controlled by regulating arc current (\( I_m \)), wirefeed speed and arc length (\( K_a \)).

Fluctuations in wirefeed speed are minimised by closed loop speed regulation of the wirefeeder motor.

Arc current and length can be controlled precisely by the choice of a suitable power source whose output can be electronically controlled in response to real-time changes in the arc status.

It has been demonstrated that the above methods have improved the Dip Transfer process performance in the following ways:

a) good welds are possible over a wider range of currents and voltages than is possible with conventional MIG welding equipment

b) fusion properties are enhanced by operating the Dip process at optimised shortcircuit and arc currents
c) cycle to cycle weld consistency is obtained by regulating the mean and instantaneous currents to within 5% of the optimum programmed levels.

d) lower spatter levels are experienced.

Spatter Reduction: Spatter on the weld results in loss of weld metal (5-10%), causes weld defects and requires costly weld-dressing for certain applications.

Some research has been carried out in the field of spatter reduction and these are summarised below (with reference to Figure 2.8):

a) It has been shown that spatter is produced by the repulsion of the molten tip at the weldpool surface, at the instant of shortcircuiting. This effect can be reduced by delaying (Td) the application of the shortcircuit current until the wire tip has embedded itself into the weldpool. The explosive detachment of the wire tip is then restrained by the surface tension of the weldpool. Typical values of Td of between 50 - 250 uS are required, depending on the wire and gas composition.

b) The explosive rupture of the molten tip at the point of arcing is also a prime source of spatter. The explosive forces are current dependent (Lorentz force), and it has been suggested that the current should be reduced to the arcing level, prior to the wire fusing, in order to reduce spatter. This is however difficult as it requires prediction of the time at which the arc will rupture.
Control unit used for Dip transfer process development

Dip transfer process waveforms showing controllable parameters

FIGURE 2.8
Detection of the rate of change of arc voltage is one possibility as this is observed as being the precursor to a rupture. In practice, this would require the control electronics to be able to discriminate between normal arcing conditions and electrical noise in the arc voltage signal.

Other researchers have overcome this problem by estimating the value of $T_p$ for the different wire/gas combinations, but this method is still very subjective.

Summary: Current controlled Dip Transfer offers advantages of less spatter and better fusion properties compared to the conventional Dip Transfer process. A further progression in this process could be made if the arc current and wire feed rate controls were consolidated into just one control (i.e. wire feed rate or $I_m$). Conventional Dip Transfer requires the operator to set three variables (wirefeed rate, arc voltage and output inductance).

2.6.2 Pulsed Current MIG (PCM)

In the PCM process, the arc is continuous but metal transfer is intermittent. Droplet detachment occurs only when the current exceeds the spray transition level during the peak pulse period - Figure 2.9a. The deposition rate is proportional to the droplet detachment frequency. By selecting suitable pulse parameters, one droplet of a given volume can be


**FIGURE 2.9a**

Schematic square wave pulse current

- $I_p$, $T_p$: pulse current and duration
- $I_b$, $T_b$: background current and duration
- $I_m$: mean current
- $T$: total cycle duration
- $I_p = I_p, I_b$: excess of pulse over background current

**FIGURE 2.9b**

Overall relationship between pulse and background currents as a function of mean current and total cycle duration.

Normalized pulse current $I_p/I_m$ vs. Normalized background current $I_b/I_m$
detached per pulse of current. If the pulse current frequency and the wirefeed speed are linearly related, the wire burnoff rate can be optimised such that a constant arc length is achieved over a 10:1 range of welding current (Im). This reduces the operator controls to just one variable (wirefeed rate).

The power source is pre-programmed to produce the required burnoff rate. This mode of PCM has been called SYNERGIC MIG and is a more general form of Pulsed Current MIG.

Using transistorised power supplies, a nominally square wave of current is easily produced in which the current amplitudes and durations can be varied independently and over a wide range. Experimental investigations into the Pulsed Current MIG process were initiated in 1970 and were conducted with Transistor Series Linear Regulator types of power sources. The main investigations were focused on:
- the determination of viable pulse parameters for a given wire and shielding gas combination
- the influence of pulse parameters on droplet size
- the influence of pulse parameters on wire and workpiece heating
- the stability of the arc during the peak and background periods; also, the effect of power source characteristics on arc stability
Pulse Current Parameters

Prediction of electrical parameters for the PCM process is possible for most wires that exhibit spray transfer properties. Certain process requirements need to be met:

(i) Wire Burnoff criteria

The wire feed rate and wire burn off rate need to be matched to maintain a constant arc length over the full range of welding currents. The relationship that represents all feasible pulse current parameters is given by Figure 2.9b:

\[ Im = \frac{Ip.Tp + Ib.Tb}{T} \]  

The spray region is extended to currents lower than the transition current level for the wire/gas combination. This "pseudo" spray condition is maintained for Im values as low as 50A. The burnoff equation is

\[ Im = Kw.W + Ki \]  

where \( W \) = wirefeed rate (metres/minute)

\( Kw \) = wire burnoff constant (Amps/metre/minute)

\( Ki \) = minimum current (Amps)

Kw,Ki both vary for wires of different sizes and composition, shielding gas and wire "stickout" length.

(ii) Metal Droplet size

In the Pulsed Spray mode, the size of the metal droplet needs to be kept constant as Im is varied.
The droplet size can be predetermined from:

\[ T_p = \frac{240 \cdot v \cdot d \cdot W}{d} \quad \ldots \ldots \quad (13) \]

where \( v \) = droplet volume
\( d \) = wire diameter
\( W \) = wirefeed rate (metres/min)
\( T_p \) = detachment time

Values of \( T_p \) can be measured for various currents and wirefeed rates and these are related by:

\[ T_p = \text{constant} \quad \ldots \ldots \quad (14) \]

This equation implies that a droplet of a stated volume will be detached for any combination of \( I_p \) and \( T_p \).

This leaves \( I_b \), \( T_b \) as the only unknowns in equation (11). \( I_b \) needs to be greater than the minimum current required for arc stability. \( T_b \) is limited to values such that:

\[ F > F_{\text{min}} \]

where \( F = \frac{1}{T_p + T_b} \)

\( F_{\text{min}} \) = the minimum pulsating arc frequency for operator comfort (\( \sim 25 \text{ Hz} \))

Discussion

The choice of parameters satisfying equation (11) and (14) will depend on the welding position employed, workpiece thickness and geometry and the required weld characteristics (bead appearance, penetration profile, etc). It has been shown that better fusion properties are obtained by selecting \( I_p \), \( T_p \) combinations that satisfy equation (14) but which are of longer duration and lower amplitude.
2.7 Arc Stability

Under certain operating conditions (e.g. low arc currents), the arc plasma will de-ionise rapidly \(< 200\text{ms}\) causing the arc to extinguish. This has been attributed to the lack of cathode spots on the workpiece for the arc to establish. This is particularly apparent at low arc currents in the Pulsed Current MIG process.

Arc outages also occur due to changes in the standoff (the torch - workpiece separation) - Figure 2.10. Constant voltage characteristic power sources are able to compensate for such perturbations (Figure 2.10C,F). The arc length will vary, under similar conditions, when a constant current characteristic power source is used. A reduced arc length could cause arc outages as a result of the wire tip shorting to the weldpool - Figure 2.11a. The arc can also extinguish if the arc length increases to such an extent that the power source is unable to supply the arc current at the increased arc voltage. Magnetic fields produced by tempered materials that are to be welded or that due to current flow in conductors near the arc are also responsible for arc instability.

2.7.1 Power Source characteristics for stable arcs

Arc instabilities are present in both C.C and C.V. controlled Pulsed MIG processes (Figure 2.11a,b). Arc outages can be prevented by restricting the arc
The Effect of Torch-Workpiece distance variation illustrated for constant current and constant voltage characteristic power sources.

**FIGURE 2.10**

- **A.** normal arc
- **B.** current constant
  - arc length reduced
- **C.** current increases
  - arc length constant

**Decreased stand-off**

- **D.** normal arc
- **E.** constant current
  - arc length increased
- **F.** current reduced
  - arc length constant

**Increased stand-off**
Arc instability occurring for pulsed current welding using constant current characteristic power sources

FIGURE 2.11a

Arc instability occurring during pulsed voltage welding using constant voltage characteristic power sources

FIGURE 2.11b

limits for Vp

peak period characteristic

area for stable arc operation

background period characteristic

stable arc operation area by applying limits to maximum and minimum arc voltages and currents

FIGURE 2.11c
current and voltages to levels that produce stable arcs. This is only possible with transistorised power sources whose output characteristic and operating points can be dynamically altered in response to arcing conditions. A stable arc can be achieved by preventing the conditions:

\[ I_b = 0, \ V_b = 0, \ V_p > V_i \]

A system for achieving this has been proposed (Figure 2.11c) where the background period is controlled by a shaped characteristic that limits \( I_b \), \( V_b \) to the minimum values consistent with stable arcs. Similarly, the peak period is operated with a shaped characteristic. The operating points for normal arc lengths are within the C.C., C.V. lines for both periods. If the arc length reduces excessively, the background voltage is maintained above the minimum voltage line by an increase in \( I_b \). Similarly, increases in arc length will restrict \( I_b \) to \( I_b \) min. The maximum voltage during the peak period is also limited if the arc length increases. This system of control has the advantages of C.C. operation, (defined, regular droplet transfer and fusion properties) with the self-adjusting arc length properties of the C.V. operation. The latter only occurs for conditions that produce unstable operating points.
2.8 Summary

The prerequisites for quality MIG welding are:

i) the generation of controlled arc parameters that influence wire melting and detachment and workpiece heating; the arc current needs to be the controlled variable in preference to the arc voltage (as is conventional practice)

ii) the controlled detachment of metal from the wire

iii) stable arc conditions

iv) reduced spatter in the Dip Transfer process by delaying the application of the shortcircuit current; fusion properties are improved by maximising the arc current for a given wirefeed rate

v) the pulsed current parameters need to be within the constraints of the fundamental equations relating to metal detachment and transfer, droplet volume size and arc stability; the successful use of this process is therefore restricted to those power sources with dynamic and static electrical characteristics that allow for the implementation of the process equations

vi) automatic regulation of the arc length is required when current characteristic power sources are employed for MIG welding
3. MIG WELDING POWER SOURCES: TECHNOLOGY REVIEW

3.1 Introduction

In arc welding, the power source supplies all of the energy consumed in the welding process. MIG welding power sources utilise a constant voltage (C.V.) characteristic, to maintain a constant arc length (which to a first order is proportional to arc voltage). This is explained by examining the interaction between the arc electrical characteristic (the load curve) and the power source characteristics - Figure 3.1. A spray arc is produced if the wire feed rate (Wo) and wire burn off rate (α Io.Vo) are equal. A momentary increase in arc length (produced, for example, by a change in joint geometry) needs to be countered by an increase in the wire stickout in order to restore the arc to its original length. This is achieved by reducing the burnoff rate. With C.V. power sources this occurs automatically. The new operating point A1 produces an arc current I1 < Io.

The wire burn off rate is now less than the wire feed rate, causing the wire to move closer to the weldpool and re-establish arc length (Lo). The additional voltage (V1 - Vo) is dropped across the increased wire stickout. The converse is true for a momentary decrease in arc length where the new operating point A2 (I2, V2, Wo) results in a higher current (I2 > Io) that melts off an extra length of wire to restore the arc length Lo.
This process of self-adjustment of the arc length is widespread in MIG welding employing C.V. characteristic power sources and is used in over 95% of MIG welding equipment designs. Excessive variation in Io, however, will result in poor weld bead fusion (if I1 << Io) or over penetration (loss of weld and plate material) if I2 >> Io.

3.1.1 Power Source Static Characteristics

Typically, flat characteristic power sources have a regulation (slope) of about 2.5V/100A i.e. a change of ±2.5V in arc voltage will result in a ±100A change in arc current to re-establish the arc length. In electronic power sources, the volt/ampere characteristic slope can be made to follow the equation

\[ m \cdot I_m + n \cdot V_m = \text{constant} \quad (m + n = 1) \quad \ldots(15) \]

where \( m \), \( n \) are constants.

Using this technique, the characteristic can be varied between constant voltage (\( m = 0, n = 1 \)) and constant current (\( m = 1, n = 0 \)) - Figure 3.2.

In high quality MIG welding, the arc current rather than arc voltage is the preferred controlled variable. Consequently, the arc length will fluctuate, but the effect on fusion properties is of a secondary nature. Arc instability due to the absence of arc length control is a major drawback of the constant current characteristic power source and a method of regulating the arc length independent of arc current is desirable.
Arc length self-adjustment mechanism for constant-voltage characteristic power sources

Variation of power source output characteristic by altering current and voltage feedback
3.1.2 Power Source Dynamic Characteristics

Two basic factors determine the response characteristics of a power source - the frequency of operation of the regulation mechanism (e.g. 50Hz or a low harmonic for phase controlled thyristors) and the output inductance. The output inductor is used as a store of electrical energy that acts as an energy buffer between the power source regulating mechanism (response > 100 us) and the arc load (response < 100 us).

A rapid increase or decrease of arc voltage is accommodated by a corresponding change in voltage across the inductor at relatively constant current, which maintains the arc. The output inductor also serves to reduce the current ripple amplitude.

3.2 Power Source Technology Review

3.2.1 General Description of MIG Power Sources

Direct Current MIG welding power sources consist of 3 basic elements:

a) Voltage Transformation from single or three phase supplies to about 35-75 V rms line voltage. Galvanic isolation from mains potential is also necessary.

b) Rectification of the transformer secondary voltage to produce a 50 - 100 V d.c. supply capable of supplying up to 500 A d.c. current into the arc.

c) A power control mechanism either on the primary or secondary side of the transformer.
Various auxiliary items like cooling equipment, instrumentation, current and voltage shunts are needed for all the above designs.

3.2.2 Types of Power Sources for MIG Welding

The main differences between the various types of power sources is in the complexity of the power control mechanism. In general, simple control methods are found in low cost sets where the quality of the weld produced is not critical.

Transformer-Rectifier sets have d.c. output voltages controlled by varying the a.c. voltage into the rectifier stage. This is achieved by voltage tappings on the primary or secondary windings of the transformer. These types of sets have the advantage of low cost but closed loop control of the output parameters are not possible.

Phase Controlled Rectifier (PCR) sets are either of the half or full controlled bridge types. The output can be closed loop controlled to produce an output that has accuracy and repeatability of the arc parameters. The current ripple is excessive particularly for low conduction angles of the thyristors. Furthermore, discontinuous load currents can occur. The output inductance is therefore designed to prevent the above from affecting the welding performance of the set. The PCR sets are used mainly for medium quality fabrication due to the higher cost of the equipment.
3.2.3 Transistor Series Linear Regulator Power Source

The transistorised Series Linear Regulator (SLR) welding power source is based on the same principles as an audio amplifier but with an output power of up to 30kW.

Operating Principle

A Series Linear Regulator power source consists of a 60 - 100V d.c. supply (obtained by mains voltage transformation and rectification) and an amplifier stage. The amplifier consists of a large number of transistors (typically 100+) connected in parallel. As the power devices are continuously passing load current, the dissipation in each device

\[ P = (V_i - V_m) \times I_m \]  

For a 500A, 60V power source, the power dissipation in the devices is between 2.5 - 17.5kW. This power loss is dissipated in a large number of transistors that need to be water cooled. The high cost of SLR power sources (£30/A) limits their use to the high quality welding market (defence, aerospace, nuclear industries).

Advantages

1. Accuracy and repeatability of setting better than 1% of maximum output

2. Full Power Bandwidth of 1kHz minimum and up to 10kHz with the use of suitable transistors and feedback sensing circuitry

3. In Pulsed current operation, rise and fall times of 250nS or better are possible
4. Flexibility of programming of arc voltage, current, pulse waveform profile etc. Output characteristics are continuously variable between C.V. and C.C.

5. Low current ripple (< 2.5 Amp @ 500A output).
   Capable of rejecting 300Hz mains ripple very effectively (-60db)

Disadvantages

1. Power efficiency varies between 20% and 55%
2. High manufacturing costs incurred in device selection, assembly and water cooling
3. The power amplifier tends to be bulky and cumbersome and the cooling system prone to leaks, blockage of the cooling channels, freezing of the coolant in low atmospheric temperatures and heavy condensation on the heatsinks in atmospheres of high humidity
4. Because of the large number of power devices used (100+), product reliability can be severely impaired and a large amount of device redundancy (up to 30%) is usually built into the design

3.2.4 Transistor Series Switching Regulator (Chopper) Power Source

In Transistor Series Switching Regulator (SSR) power sources, the transistor switch is either fully conducting (or blocking) the passage of current from the supply to the load. Whilst the principle is well established, the earliest published information on its use in welding power sources was for TIG welding.
Operating Principle

As in the case of the SLR power source, the chopper amplifier operates from a low voltage (60 - 100V d.c.) supply with capacitive filtering (Figure 3.3a).

A bank of power transistors is connected between the d.c. supply and the arc load. The transistors are switched between their conducting and blocking states at a frequency between 2 - 20kHz. When the transistors are conducting, diode Df is reversed biased and the supply voltage is applied to the inductor Lf. The current in the inductor and load increase at a rate

\[
d(iL/dt) = (V_i - V_m)/L_f
\]

At the end of the conduction period, the transistors are switched off and the load current flows in Df and Lf. This results in an exponential decrease in the load current until the transistors are switched "on" again.

Typical load current waveforms (pulsed load) are shown in Figure 3.3b for a 2kHz transistor chopper set. The ripple amplitude is inversely proportional to the choice of modulating frequency (2 - 20kHz) and inductance Lf. In selecting the modulating frequency, the following need to be considered:

a) Response time:

The response time is determined primarily by inductance Lf. Typically, Lf values of < 100 uH will yield response times of < 0.5 ms. The minimum value of Lf is that which will produce stable arc conditions (\( \geq \) 25uH). The modulation frequency (Fo) is then selected to minimise arc acoustic noise (Fo > 15kHz). Lower values of Fo will
Circuit and waveforms for a Series Switching Regulator ('Chopper')

Arc load
(V_n, I_m)

FIGURE 3.3a

Arc current (pulsed reference) waveform for a low frequency transistor chopper power source
require higher values of \( L_f \) in order to suppress the current ripple amplitude and this in turn will increase the response time.

b) Current Ripple Amplitude:

For reproducible performance, the current needs to be regulated to better than 2.5% of the set value. The ripple in the output can result in poor definition in the output and hence needs to be minimised. For a given modulating frequency, the inductance is selected to give an acceptable ripple amplitude (< 5A) and response time. Some compromise between these requirements is generally necessary.

c) Ripple Frequency:

This is also important for acoustic reasons. The 28 arc has a wide bandwidth and will reproduce any frequency within the audible range. The acoustic emissions from the arc can have a detrimental effect on operator performance. The modulating frequency should be greater than 15kHz or less than 2kHz.

Power dissipation in the transistors is less than 5 Watts/Ampere output (c.f. up to 35W/Ampere for Series Linear Regulators). The availability of high current (300A) transistors has simplified the design of switching regulator power sources and a typical 500A set could have 4 - 6 devices in parallel. The limited availability of fast switching devices had restricted modulating frequencies to less than 5kHz.

Advantages
(These are based on the proposed design of power source).
1. Accuracy and repeatability of setting better than 2% of output

2. Full power bandwidth of 500Hz maximum ( @ 20kHz modulating frequency)

3. Flexibility of programming of arc parameters, output characteristics etc

4. Current ripple amplitude of less than 10A

5. Full load efficiency better than 75%

6. High input power factor due to full-wave rectification of input supply.

Disadvantages

1. Moderate cost (£10/A) but still expensive when compared against conventional welding equipment (£2.50/A)

2. Complex electronics required for the control of the power transistors and the PWM waveforms. This can reduce the reliability of the power source

3. The switching regulator draws current from the mains supply intermittently and this produces EMI and RFI which need to be suppressed to meet statutory electrical noise regulations (e.g. VDE 0871)

The limiting factor in the design of MIG welding sets, using the chopper principle, is the availability of power switching devices capable of withstanding the arduous conditions present in the process (e.g. repetitive shortcircuiting of the power source output). For operation at high modulating frequencies (> 15kHz), power transistors with fast switching characteristics (e.g. switching times < 1.0 us @ 300A) are required.
For this reason, the chopper based welding power sources, to date, have been limited to those operating at low modulating frequencies.

3.2.5 Primary Inverter type of Power Source

Over 95% of fabrication welding can be satisfactorily carried out using Transformer-Rectifier or Phase Controlled Thyristor sets. The market for high quality welding sets is small and has limited potential for growth unless equipment costs are reduced.

The primary inverter design has been propounded for a number of years as being the most cost effective method of electronic control of the welding process.

Operating Principle

The primary inverter consists of four elements of power control - Figure 3.4a:

- a rectifier which converts single or three phase supplies into a d.c. supply (300 - 600V)
- an a.c. transformer operating at the inverter frequency (2 - 25kHz) provides primary-secondary isolation and voltage reduction
- rectification of the output to a d.c. supply

The only differences in the designs used are in the inverter stage where the variables are circuit topology, power devices and the method of closed loop control (fixed and/or variable frequency with pulsedwidth modulation). The simplest and cheapest designs are based on the half bridge inverter circuit - Figure 3.4b.
Operating Principles

Transistor switches TR1 and TR2 and diodes D1 and D2 are the main switching devices in the inverter circuit. During the positive half cycle of operation, TR1 is switched on causing current to flow from the supply into Lp and C1, C2. This produces a corresponding flow of current in the secondary winding of the transformer into the load circuit. When TR1 is turned off, D2, D3, D4 maintain the flow of current in Lp, Lf. TR2 is turned on at the start of the second half cycle and the current in Lp is now reversed. D1, D3, D4 flywheels the current in Lp, Lf when TR2 is turned off. The current flow in the load is unidirectional due to the rectification diodes D3, D4. The conduction time of TR1 and TR2 is pulsewidth modulated to achieve control of the output current/voltage. The following considerations are required in the design of the inverter:

a) Power devices:

These need to be rated for a minimum value of rectified mains supply, have fast switching times (1μs) and low on-state losses for operation at 20kHz. The specification can be relaxed for operation at lower frequencies (2kHz).

The secondary rectification diodes must have fast reverse recovery characteristics and be of a low recovered charge type.
b) Power Transformer:

The power handling capability of a transformer can be quantitatively expressed as:

\[
P = K \times K_m \times \text{Vol.} \times F \quad \ldots \ldots \quad (18)
\]

where

- \( K \) = Constant
- \( K_m \) = Core Material Constant
- \( \text{Vol.} \) = Volume of Material
- \( F \) = Frequency of Transformation

Iron cored materials are used at up to 2kHz modulating frequency, above which the eddy current and magnetic hysteresis losses are high and cause an excessive temperature rise in the cores.

For power transformation above 10kHz, ferrite cores are used due to their low core loss properties.

This however is offset by their poor thermal conductivity which limits the usable frequency to less than 50kHz for high power transformation.

The reduction in volume of the transformer material with increased frequency is evident from equation (18).

Advantages:

1. Reduced size and weight compared to conventional equipment employing 50 Hz transformers
2. The power sources are portable and transportable
3. High output specification possible if modulating frequencies greater than 15kHz are used

Disadvantages:

1. Relatively sophisticated electronics which will require additional personnel training for field servicing and maintenance
2. Less reliable than low voltage systems and susceptible to mains borne transients

3. Typical costs of £5 - £7.50/A puts this technology of power source into the "up market" sector at the present time

3.2.6 Choice of Technology for future designs of Power Sources

Higher technology power sources will be used increasingly in automatic, mechanised and high quality semi-automatic MIG welding. However, the end user costs for high technology sets will need to be reduced from the present £30/A for Series Linear Regulator designs to less than £10/A. This compares with a cost of £2.50-£5/A for the sets available for general fabrication.

The high frequency primary inverter and secondary switched regulator (chopper) are the only power circuit topologies that could be considered for the design of high specification welding power sources that meet the marketing cost target of £10/A.

The high frequency transistor chopper was selected for development for the following reasons:

a) The development risk was assessed to be lower for the chopper design due to the availability of power components that were past their development phases.

b) Market research indicated that a product was required within 2-3 years. This would not have been possible with the complexities of inverter designs.
c) The chopper design is viewed as an evolutionary product as it shares the Transformer-Rectifier stages of its predecessors. Consequently, it would be easier to train the end user to service and maintain the sets. It could also be viewed as the near ultimate (Series Linear Regulators being the ultimate) in performance in secondary controlled power source designs.

d) The low frequency (< 5kHz) chopper power sources introduced to the market were readily accepted by the market. In comparison, the low frequency inverters introduced in the early 1980's were renowned for their unreliability.

3.3 Specification for the Proposed Chopper Power Source

Input supplies: 380 - 440V rms, 50/60 Hz

Isolation type: star (primary) - delta secondary transformer

Output Ratings
(d.c.): Open circuit voltage 65V

Full load voltage 40V @ 500A

Short circuit current 500A

Full load current 350A @ 100%

500A @ 60%

Ripple current amplitude < 5A p/p

Power bandwidth > 500 Hz

Output regulation -
constant current mode 5A/50V
constant voltage mode 0.5V/100A

Efficiency > 75%
Input power factor   > 0.8

Process capabilities:
Constant current characteristic
Dip and Pulse Spray MIG welding
of mild and stainless steel wires
Incorporation of a secondary
control loop to regulate the
arc length
4. THEORETICAL ANALYSIS AND COMPUTER MODELLING OF THE HIGH FREQUENCY TRANSISTOR CHOPPER CIRCUIT

4.0 Introduction

Previous computer models of the chopper power circuit were based primarily on the analysis of the commutation circuits of the main thyristor switch. The effects of circuit stray inductances and capacitances were of lesser importance as the switching frequencies were of the order of a few kilohertz. In the design of the proposed transistorised chopper, the effects of circuit impedances cannot be ignored due to the fast switching times (< 1μs) of the transistors and the high modulating frequencies (> 15kHz) used. Furthermore, the welding arc presents the chopper circuit with a load that can vary rapidly between 10 milliohm and 1 kilohm.

The model described in this chapter is unique in that it is capable of optimising circuit component values, predicting the circuit performance into dynamic loads and enables the selection of power devices for the application. In this respect, the computer model developed is a major contribution to the present state of knowledge in the field of power electronics.

4.1 Transistor Chopper Power Module

4.1.1 Circuit Description

A simplified circuit for the series switching regulator (chopper) is shown in Figure 4.1a. It consists of three basic sections:
a) the unregulated d.c. voltage supply - \( V_i \)
b) a high frequency transistor switch (\( TR \))
c) an output filter (\( L_f \)) and load (\( V_L, R_L \))

Circuit operation is best described with reference to Figure 4.1a and 4.1b.

Assume that prior to the transistor being turned on, that current is flowing in the load \( R_L, V_L \) through flywheel Diode (\( D_f \)) and output filter inductor (\( L_f \)).

When \( TR \) is turned on, the current in \( D_f \) is commutated to it. The current in \( L_f \) increases until the transistor is next turned off. During this interval, power transfer takes place between the d.c. supply and the load. When \( TR \) is turned off, its current is transferred to diode \( D_f \) during the transistor current fall time. Thereafter, the current in the load decays in a loop composed of \( D_f \) and the load. To operate as a current source supply, current feedback is employed in the control loop. The period of transistor conduction and modulating frequency will vary dependent on the demand and load conditions.

4.1.2 Types of Chopper Regulators

The duty cycle (\( T_{on}/T \)) of the chopper can be altered using the following modulation strategies:

a) variable frequency, fixed pulse width - Figure 4.2a
b) variable frequency, fixed off-time - Figure 4.2b
c) fixed frequency, variable pulse width - Figure 4.2c

In Method (a), the frequency is varied in direct response to the output load conditions. The advantage
Simplified circuit for a current source chopper

FIGURE 4.1a

Typical waveforms for the chopper circuit

FIGURE 4.1b
Various Pulse Width Modulation Techniques

(a) Fixed Pulse Width, variable frequency

(b) Fixed Off Time, variable frequency

(c) Fixed frequency, variable Pulse Width
of a fixed pulsewidth is that the power transistor can be allowed to saturate and discharge all circuit capacitances and inductances prior to being switched off. Furthermore, the switching losses are minimised at all loads since the frequency of operation is 6 optimised to the load ripple, the latter remaining constant for all load conditions.

In Method (b), the transistor on-time is varied and the off-time is fixed. This produces a decrease in frequency with increasing loads. Characteristics of this type are useful where power dissipation needs to be minimised at high loads. Transistor and flywheel diode switching losses will therefore decrease as the load increases. A trade off between increasing saturation losses and decreasing switching losses is required.

Method (c) employs Pulse Width Modulation (PWM) control techniques where the transistor conduction time is increased in proportion to the load demand. The advantage of this system is that the analysis and calculation of circuit component values and device losses are easily predicted from computer models. The main disadvantage is that the devices are switched at high frequencies under all load conditions which reduces overall system efficiency. Method (c) was preferred to the other methods as it would produce less acoustic noise in the arc if the modulation frequency was chosen to be higher than the audible threshold.
4.2 Analysis of the PWM Transistor Chopper Circuit

The simplified circuit of Figure 4.1a needs to be modified considerably to obtain a practical system. This requires the addition of protection circuitry around the power devices and for stray capacitances and inductances to be considered. The circuit of Figure 4.3a has been derived for use on the computer model.

A set of time dependent voltage and current equations can be written from Figure 4.3b. These are inter-related and for this analysis, the current equations are treated as the primary variables and the voltages at various points in the circuit and across certain circuit elements are derived thereof. The currents $i_c$, $i_S$, $i_z$, $i_F$, $i_T$ and $i_L$ are analysed for each time period and used to evaluate the voltages $U_{ce}$, $U_L$, $U_k$, $U_s$. The voltage equations below are written with reference to Figure 4.3b,

\[
U_c = V_i - L_c \frac{d(i_c)}{dt} \quad \text{....(19)}
\]

\[
U_e = U_c - U_z, U_c - U_p \text{ or } U_c - U_t \text{ (depends on the state of } D_z, C_s, T_R) \quad \text{....(20)}
\]

\[
U_{ce} = U_c - U_e \quad \text{....(21)}
\]

\[
U_k = U_e - L_{xe} \frac{d(i_c)}{dt}
\]

\[
= -[U_f + L_{xf} \frac{d(i_F)}{dt}] \quad \text{....(22)}
\]

\[
U_L = V_L + R_L i_L = U_k - L_f \frac{d(i_L)}{dt} \quad \text{....(23)}
\]

\[
U_z = V_z + R_z i_z \quad \text{....(24)}
\]

\[
U_p = U_s + L_{xs} \frac{d(i_S)}{dt} \quad \text{for } i_S > 0 \quad \text{....(25)}
\]
Chopper power circuit inclusive of stray impedances and protection circuitry

FIGURE 4.3a

Chopper circuit adapted for computer modelling

FIGURE 4.3b
\[ U_p = U_s + R_s i_S + (L_s + L_{xs}) \frac{d(i_S)}{dt} \]

for \( i_S < 0 \) .... (26)

\[ U_s = \frac{1}{C_s} \int i_s \, dt \] .... (27)

For the purpose of this analysis, mathematical idealised switches \((K_n)\) are inserted into the circuit, the subscript \((n)\) defined by the location of the switches e.g. \(K_t =\) transistor switch.

Switches \(K_n\) are then opened or closed depending on whether a particular device needs to be isolated from the analysis.

4.3 A detailed examination of the predicted current waveform for the circuit (Figure 4.4) reveals nine time periods \((I - IX)\) for each cycle of operation at the modulating frequency \((F_0)\). In the analysis, the equations for circuit currents and voltages for all nine periods are derived in Appendix A. These are summarised below for reference purposes.

Summary of circuit analysis

It is assumed that the circuit has been operating for at least one cycle and that current has been established in \(L_f\) and the load \((R_L,V_L)\). After \(T_R\) has been turned off in Period V, the circuit attempts to attain steady state conditions in preparation for the start of the next cycle. For example, \(L_c\) acts as a \(di/dt\) limiter of transistor current at the start of a cycle and hence needs to be fully discharged before the end of the previous cycle in order to be effective at the start of the next cycle.
This can only be attained if Toff is long enough to allow the circuit to attain steady state conditions. Otherwise the circuit will be in a transient state at t₀ when TR turns on.

The initial conditions for the circuit variables for the next cycle are determined by the circuit status at t₀ (one of Periods VI, VII, VIII or IX of the previous cycle). The variables need to be evaluated and stored as constants e.g. Ic56 = current in Lc if t₀ occurs during Period VI of the previous cycle.

Circuit Operation during the new cycle (n):

4.3.1 Period I - t₀ < tₙ < t₁

With reference to Figure 4.5, when TR turns on,
- Cs begins to discharge through Ls, Rs and TR
- Df forward current begins to transfer to TR until IF = 0 at t = t₁, which marks the end of Period I.
- load current remains constant [load discharge time constant >> (t₁ - t₀)]

Summary of Period I Equations

\[ i_{st} = - \frac{(V_s - U_t) \sin[X₃, t]}{L₃, X₃} \exp\{\frac{-Rs, t}{2, L₃}\} \ldots(28) \]

\[ IF = I_{fo} + \frac{(U_t - V₁ - U_f), t}{(L_{xe} + L_{xf} + L_c)} \ldots(29) \]

\[ iL = \text{constant} \]

\[ ic = ic(t₀) + (iL - IF) \ldots(30) \]

\[ iT = ic + i_{st}; \text{if } ic(t₀) > 0 \ldots(31) \]

\[ iT = i_{st} + (iL - IF); \text{if } ic(t₀) < 0 \ldots(32) \]

\[ U_{ce} = U_{ce}(t₀) \left(1 - \frac{t}{Tr}\right) \text{for } t < Tr \ldots(33) \]

\[ U_{ce} = Ut \text{for } t > Tr \ldots(34) \]
Us = -(Vs-Ut).\left[ X3 - \sqrt{1 \cdot \exp(-Rs \cdot t) \sin(X3 \cdot t + X4)} + Vs \right]_X3 \left[ \frac{1}{VL3 \cdot Cs} \right] \left( \frac{2 \cdot L3}{L} \right) ....(35)

4.3.2 Period II - t1 < tn < t2

The minority carrier charges in Df are removed by a flow of negative current in the diode (Figure 4.6a). When iF = Irm (Figure 4.6a), the forward recovery of Df is completed and this marks the end of Period II. The discharge of Cs continues; IL increases linearly.

Summary of Period II Equations

\[ Qrr = \frac{1}{2}(tfr + trr) \cdot Irm \] ....(36)

\[ tfr = \sqrt{\frac{3 \cdot Qrr}{(1 + S) \cdot \frac{d(iF)}{dt}}} \] ....(37)

\[ Irm = - \frac{(Vi + Uf - Ut) \cdot tfr}{(Lxe + Lxf + Lc)} \] ....(38)

\[ i_{st} = \text{equation (28)} \]

\[ iF = \text{equation (29)} \]

\[ iL = \left[ \frac{2Vi - VL}{RL} \right] + \left[ \frac{iFo - (2Vi - VL)}{RL} \right] \cdot \exp\left[ -\frac{RL(t - t1)}{L_f} \right] \] ....(39)

\[ \text{ic} = iL - iF \]

\[ iT = \text{ic} + i_{st} \] ....(40)

\[ Uce = Ut \]

\[ Us = \text{equation (35)} \]

\[ UL = VL + iL \cdot RL \] ....(41)

4.3.3 Period III - t2 < tn < t3 (Figure 4.6 a,b)

The negative flow of current in Df reduces from its peak value to zero in time trr, and Df attains its full blocking status at t = t3. During Period III, the discharge of Cs continues; load current IL increases linearly.
Circuit conditions during Period I
FIGURE 4.5

Details of Df reverse recovery
FIGURE 4.6a

Circuit conditions for Periods II & III
FIGURE 4.6b
Summary of Period III Equations

\[ \text{i}^\text{st} = \text{equation (28)} \]

\[ \text{iF} = \text{Irm. } [(\text{t}-\text{t}_2) - 1] \text{ for } \text{iF} < 0 \text{ only } \ldots(42) \]

\[ \text{iL} = \text{equation (39)} \]

\[ \text{ic} = \text{iL} - \text{iF} \]

\[ \text{iT} = \text{equation (40)} \]

\[ \text{U}_{\text{ce}} = \text{Ut} \ldots(34) \]

\[ \text{Us} = \text{equation (35)} \]

\[ \text{UL}^* = \text{VL} + \text{iL.RL} \ldots(41) \]

4.3.4 Period IV - \( \text{t}_3 < \text{t}_n < \text{t}_4 \)

The duration of Period IV is determined by the pulse-width (PW) for this cycle of operation. During this time and with reference to Figure 4.7

- \( \text{iL} \) continues to increase
- \( \text{Cs} \) initial discharge is completed
- \( \text{Cs} \) then charges and discharges resonantly due to the underdamped nature of the snubber circuit

For the half cycle when \( \text{Cs} \) is charging, the load current is supplied partly by \( \text{Cs} \). As the current in \( \text{Lf} \) is virtually constant over the short resonant time period, \( \text{iT} \) decreases such that

\[ \text{iT} + \text{iS} = \text{iL} \quad \ldots(43) \]

Summary of Period IV Equations

\( \text{i}^\text{st} \) is given by (28) until \( \text{i}^\text{st} = 0 \); underdamped resonant charging of \( \text{Cs} \) (current \( \text{i}_{\text{sl}} \)) then occurs giving
is1 = \[\frac{V1 + Us(n) - VL}{L2.X2} \sin(X2.(t-ta).\exp[-RL(t-ta)]\] 
\[\frac{2.L2}{2} \]  
\ldots(44)

when is1 = 0, the resonant discharge of Cs commences and is given by ist.

\[ist = \frac{[Us(n+1) - Ut]. \sin(X3.t).\exp[-Rst]}{L3.X3} \] 
\[\frac{2L3}{2} \]  
\ldots(45)

iF = 0

iL is given by (39)

ic = iL  \ldots(46)

iT = ic + ist if ist < 0  \ldots(47)

iT = ic - isl if ist > 0  \ldots(48)

Uce = Ut  \ldots(34)

Us is given by (160), (161), (162) of Appendix (A3.4)

UL = VL + iL - RL  \ldots(41)

### 4.3.5 Period V - t4 < tn < t5 - Reference Figure 4.8

At tn = t4, TR receives a turn-off signal and its collector current decreases to zero.

The current in Cs increases in sympathy to maintain the load current and in doing so, Cs dv/dt limits the voltage across TR.

The load current remains constant during this period.

**Summary of Period V Equations**

\[ist = iT \]  \ldots(49)

iF = 0

iL = constant = iL (at t = t5)  \ldots(50)

\[iT = IT4 \[1 - \exp\left\{\frac{-5(t-t4)}{Tf}\right\}\] \]  \ldots(51)

\[Uce = Us(n)+(Lxs.IT4.5/Tf).\exp[-5(t-t4)] \exp\left\{\frac{-5(t-t4)}{Tf}\right\}\ldots(52)\]
$$Us = Us4 + 1 \frac{(t-t4)(IT4+IS4)+Tf.IT4.exp[-5(t-t4)]}{Cs} \frac{5}{Tf}$$

..(53)

$IT4, Us4, IS4$ are values of $IT(n), Us(n), IS(n)$ at $t = t5$ i.e. at the end of Period IV

4.3.6 Period VI - $t5 < tn < t6$ - Reference Figure 4.9

TR is now in its blocking state. Cs continues to charge from the energy stored in $Lc$ and circuit stray inductance. Df remains reverse biased until $IS < iL$ which then causes Df to conduct such that

$$iS + IF = iL$$

...........(54)

The voltage across TR has increased above $V1$ and if $Vce > Vz$, then Dz conducts and diverts ic from Cs. iz > 0 marks the end of Period VI.

If $Vce < Vz$ at all times, then Period VII, VIII and IX do not occur. The circuit behaviour is then as for Period VI until TR turns on again in the next cycle.

Summary of Period VI Equations

$$isl = IL5.cos \omega(t - t5) \quad ....(55)$$

$$iF = iL - ic \quad ....(56)$$

$$iL = \frac{-(Uf+VL)+[IL5+(Uf+VL)].exp[-RL(t-t5)]}{RL} \frac{5}{2(Lxf+Lf)}$$

$$ic = isl \quad ....(58)$$

$$iT = 0 \quad ....(59)$$

$$Uce = Vs5 + \frac{IL5(1 + Cs.\omega.Lxs)Sin(\omega(t-t5))}{Cs.\omega} \quad ....(60)$$

$$Us = Vs5 + \frac{IL5.Sin(\omega(t-t5))}{Cs.\omega} \quad ....(61)$$

$$UL = VL + RL.iL \quad ....(62)$$
4.3.7 Period VII - $t_6 < t_n < t_7$ Figure 4.10

Lc continues to discharge its energy into Dz and Rz. The voltage across TR is given by $U_{ce} = V_z + I_z R_z$. The energy stored in the snubber stray inductance is discharged in $R_s$. Period VII ends when $i_S = 0$. $i_z$ is now at its maximum level.

**Summary of Period VII Equations**

\[
iz = Icz - (t-t_6) \left[ \frac{2.V_z - Icz.Rz}{2.Lxs} \right] \text{exp} \left[ \frac{-Rz(t-t_6)}{2.Lxs} \right]\\
\]

**Equation (63)**

\[
i_F = i_L - ic\\
i_L = \text{equation (57)}\\
\]

\[
ic=(V_1-V_z)(1-\text{exp}\left[ \frac{-Rz(t-t_6)}{Rz} \right]+Icz.\text{exp}\left[ \frac{-Rz(t-t_6)}{[(Lc+Lxe+Lxf)]} \right])\\
\]

\[
\text{Rz} \left( \frac{[(Lc+Lxe+Lxf)]}{[(Lc+Lxe+Lxf)]} \right)\\
\]

\[
... (64)\\
\]

\[
U_{ce} = V_z + R_z.I_z\\
\]

\[
UL = VL + i_L R_L\\
\]

4.3.8 Period VIII $t_7 < t_n < t_8$ Figure 4.11

During this period, the energy stored in Lc is completely dissipated ($ic = 0$) in Rz, Dz. $i_L$ decays in the loop composed of $D_f$, $L_f$ and $R_L$, $VL$. $ic = iz = 0$ marks the end of Period VIII.

**Summary of Period VIII Equations**

\[
is = 0\\
\]

\[
ic = \text{equation (64)}\\
\]

\[
i_F = i_L - ic\\
\]

\[
i_L = \text{equation (57)}\\
\]

\[
iz = ic\\
\]

\[
U_{ce} = V_z + R_z.iz\\
\]
Dz in partial conduction

Dz in full conduction

transfer of iC from snubber circuit to Dz

Circuit conditions for Period VII
4.3.9 Period IX - t8 < tn < t9

Cs has been charged during Period VI such that Vs > Vi. This differential voltage sets up a resonant cycle of current flow (Figure 4.12 a,b) which reduces Vs to Vi, at which point the resonant current flow ceases. iL continues to decay. Period IX ends when \( T = \frac{1}{F_0} \)

Summary of Period IX Equations

\[
\text{isf} = \left[ Us(2p-1)-Vi-Vf \right] \sin(Xk.(t-t8)). \exp[-Rs.(t-t8)] \frac{Lk}{Xk} \frac{2Lk}{Xk} \ldots (68)
\]

for the resonant discharge period

\[
\text{isl} = Vi + Us(2p) \sin[wm.(t-\tau)] \frac{Ly}{wm} \ldots (69)
\]

for the resonant charging period

\[
iC = \text{isl} \text{ or } iC = \text{isf} \ldots (70)
\]

iF = iL - ic

iL = equation (57)

Uce and Us are given by (205), (207) respectively from Appendix (A3.9).

\[
UL = VL + iL.RL
\]

4.4 Digital Computer Model of the Transistor Chopper

In order to verify the analysis of section 4.3, the equations were evaluated for different conditions of the chopper operation. The data generated was then used to predict the performance of the chopper under static and dynamic load conditions and also used as an aid to the selection of power components.

4.4.1 Programme Description

The flow chart of Figure 4.13 shows the single cycle operation of the programme. The data file "Preset"
Circuit conditions for Period VIII

FIGURE 4.11

Circuit conditions for Period IX
(snubber discharging)

FIGURE 4.12a

Circuit conditions for Period IX
(snubber charging)

FIGURE 4.12b
START

OPEN DATA FILE
OPEN PRESET DATA FILE
READ PRESET DATA FILE
CALCULATE REGULARLY OCCURRING VARIABLES

PERIOD VI

T = T + TK5
EVALUATE PERIOD VI EQUATIONS
IF UCE>Vz END PERIOD VI
ELSE CONTINUE TILL T=1/Fo
THEN SAVE PERIOD VI TIME, TK6
WRITE DATA TO DATA FILE

PERIOD I

T = 0
IF iL=0, SKIP PERIOD I,II,III
ELSE
CALCULATE PERIOD I EQUATIONS
IF iF < 0, END PERIOD I
SAVE PERIOD I TIME,TK1
WRITE DATA TO DATA FILE

PERIOD II

T = T + TK1
EVALUATE PERIOD II EQUATIONS
IF T>TK1 + TFR END PERIOD II
SAVE PERIOD II TIME,TK2
WRITE DATA TO DATA FILE

PERIOD III

T = T = TK2
EVALUATE PERIOD III EQUATIONS
IF iF = 0, END PERIOD III
SAVE PERIOD III TIME,TK3
WRITE DATA TO DATA FILE

PERIOD IV

T = T + TK3
EVALUATE PERIOD IV EQUATIONS
IF T>PULSE WIDTH END PERIOD IV
OR IF iL > Iref END PERIOD IV
SAVE PERIOD IV TIME,TK4
WRITE DATA TO DATA FILE

PERIOD V

T = T + TK4
EVALUATE PERIOD V EQUATIONS
WHEN iT = 0, END PERIOD V
SAVE PERIOD V TIME TK5
WRITE DATA TO DATA FILE

PERIOD VII

T = T + TK6
IF VCE<Vz GO TO PLOT ROUTINE
ELSE
EVALUATE PERIOD VII EQUATIONS
IF iC = 0, END PERIOD VII
SAVE PERIOD VII TIME TK7
WRITE DATA TO DATA FILE

PERIOD VIII

T = T + TK7
IF VCE<Vz GO TO PLOT ROUTINE
ELSE
EVALUATE PERIOD VIII EQUATIONS
IF iZ = 0 END PERIOD VIII
SAVE PERIOD VIII TIME TK8
WRITE DATA TO DATA FILE

PERIOD IX

T = T + TK8
EVALUATE PERIOD IX EQUATIONS
IF T = 1/Fo END PERIOD IX
SAVE PERIOD IX TIME,TK9
WRITE DATA TO DATA FILE

CALL TEXTRONIX PLOT ROUTINE
PLOT DATA
END
RETURN

START PERIOD VI

T = T + TK5
EVALUATE PERIOD VI EQUATIONS
IF UCE>Vz END PERIOD VI
ELSE CONTINUE TILL T=1/Fo
THEN SAVE PERIOD VI TIME, TK6
WRITE DATA TO DATA FILE

PERIOD I

T = 0
IF iL=0, SKIP PERIOD I,II,III
ELSE
CALCULATE PERIOD I EQUATIONS
IF iF < 0, END PERIOD I
SAVE PERIOD I TIME,TK1
WRITE DATA TO DATA FILE

PERIOD II

T = T + TK1
EVALUATE PERIOD II EQUATIONS
IF T>TK1 + TFR END PERIOD II
SAVE PERIOD II TIME,TK2
WRITE DATA TO DATA FILE

PERIOD III

T = T = TK2
EVALUATE PERIOD III EQUATIONS
IF iF = 0, END PERIOD III
SAVE PERIOD III TIME,TK3
WRITE DATA TO DATA FILE

PERIOD IV

T = T + TK3
EVALUATE PERIOD IV EQUATIONS
IF T>PULSE WIDTH END PERIOD IV
OR IF iL > Iref END PERIOD IV
SAVE PERIOD IV TIME,TK4
WRITE DATA TO DATA FILE

PERIOD V

T = T + TK4
EVALUATE PERIOD V EQUATIONS
WHEN iT = 0, END PERIOD V
SAVE PERIOD V TIME TK5
WRITE DATA TO DATA FILE

Single Cycle Programme Flow Chart

FIGURE 4.13
contains all the constants (or time invariables) of the equations derived in the analysis. These constants can be updated prior to running the programme and provides for a "what if" type of interrogation of the model to variations in supply voltage (V1), leakage inductances (Lxe, Lxf) etc. Circuit time dependent variables (ic, iI, IF, Uce, Us, etc) are evaluated every 250 ns and the data stored. The flow chart of the model equations was implemented using Fortran IV Version V31-23 on a DEC VAX-11 mainframe computer (Open University). The data was plotted on a Tektronix flat bed plotter, using Tektronix plotting software packages. The programme listing is given in Appendix A.

4.4.2 Single Cycle, "Open loop" operation of the model programme

The single cycle model is run for a period of 66 uS maximum and calculates data every 250 ns. The open loop model provides a qualitative assessment of the shape of the waveforms to be expected at various points in the power circuitry. Typical initial values have been assumed for the following variables ic, IF, iL, iS, iI, iZ, Uce, Us, UL (Figure 4.14) [In a closed loop situation, all these are set to zero (or V1) at the start of the programme]

Results

A sample of the data generated for a typical programme "run" is given in Figure 4.15. Some of the pertinent
Preset data for the open loop operation of the chopper computer model

FIGURE 4.14
A typical print of data produced by the model

FIGURE 4.15
points in the cycle are summarised below from the full data presented in Appendix A.

At [Time T (us)]

T = 0  all the variables are set at their initial conditions

T = 0.25  Uce = 1.5 Volts showing the transistor has switched from the blocking to the conducting state

T = 4.25  the flywheel diode (Df) current has decreased to zero (end of Period I)

T = 5.0  Df forward recovery complete - end of Period II. The transistor current iT is also at its maximum at this point

T = 5.5  Df reverse recovery complete - end of Period III

T = 6.50  Us = -0.76, indicating that snubber capacitor Cs has fully discharged. Note that iS is still negative and is resonantly charging Cs to the opposite polarity.

T = 11.50  iS resonant charging current is zero and Cs then commences to discharge through the load.

T = 16.75  load current iL = 250.19 and exceeds the reference current Iref = 250A.

The transistor ON Time is ended and this marks the end of Period IV. (Actual pulsewidth = 16.75 uS compared to the preset value of 35 uS; IL > 250A condition overrides the preset conditions for the pulsewidth)
T = 16.75 to 17.75

i_T has discharged to zero in 1.0 μs.

The load current has been transferred to the snubber circuit.

i_S increases to maintain i_T + i_S = i_L

C_s is rapidly discharged from its previous state and is then charged by i_S.

Period V ends at T = 17.75 μs

T = 18.0

D_f starts to conduct as i_S decreases and this ensures that i_F + i_S = i_L

T = 19.75

U_{ce} exceeds V_Z (= 120V), the level at which the protection zener conducts (end of Period VI)

T = 20.25

The zener current i_z, i_S and i_F supply the load current until i_S = 0 (end of Period VI). i_z is then at its peak level.

T = 20.0 to 22.5

i_z decreases, i_F increases and the commutation of all load current to D_f occurs when i_z = 0 (end of Period VIII). Note that the voltage across the transistor (U_{ce}) has increased above 120V. This is due to the voltage dropped across R_z = i_z.R_z

T = 22.75 to 66.0

The load current flywheels through D_f and decreases from 250.19 to 230.86 (ripple of 19.33A). C_s discharges from U_s = 132.62 to 60.0V, the supply voltage, at which point a low level of discharge continues. i_F peaks at T = 27.25 μs (290.47A). The programme is terminated at T = 66.0 μs (F_o = 15kHz).
Waveform Plots

Figures 4.16 - 4.21 are plots of the data obtained. In Figure 4.19, a voltage transient is observed during the transistor turn off period. This has been expanded in Figure 4.21 and shows that the snubber capacitor does not dv/dt limit the voltage across the transistor during the current fall time. This has been analysed as being due to the self inductance of the capacitor and snubber circuit + transistor emitter circuit inductances. The actual and predicted Safe Operating Area of the transistor is shown in Figure 4.20. The device operates within its D.C. operating boundary except for a short period during its turn on phase when the current exceeds the maximum allowable.

With reference to Figure 4.16, the transistor current reaches a peak at the point of maximum reverse recovery current flow in Df. The discharge of Cs also makes a contribution to iT during this period. The current in Dz is shown on the same trace as iT.

An expanded trace of the transistor current at turn on (Figure 4.17) shows the effect of di/dt limiting by Lc during the first 5us of operation. The snubber voltage and current waveforms are shown in Figures 4.17.

Summary

Four important observations have been made in the waveforms plotted:

a) the transistor current reaches a maximum during the first 5us of operation due mainly to the reverse recovery of flywheel diode Df
Plots of the data produced for the open loop operation of the model

(a) full cycle

(b) waveforms during transistor turn on

(c) voltages across circuit elements

FIGURE 4.16

FIGURE 4.17

FIGURE 4.18
Plots of the data produced for the open loop operation of the model

(d) full cycle
FIGURE 4.19

(e) safe operating area - predicted
FIGURE 4.20

(f) waveforms during transistor turn off
FIGURE 4.21
b) the turn off waveforms indicate that the self
inductance of Cs and its associated wiring (across
TR) inductance gives rise to a voltage transient
during the current fall time that reduces the
effectiveness of the snubber circuit.

c) the voltage across the transistor (Vce) reaches
132V (for V1 = 65V) after the transistor is in its
blocking state. This is due to the Lc - Cs resonance.

d) SOAR boundaries are exceeded transiently at turn on

4.4.3 Closed Loop Operation of the Model Programme

The closed loop control system schematic for the
current source chopper is shown in Figure 4.22.
The arc current is the controlled parameter.

(i) Control System Analysis

With reference to Figure 4.22, the current error is
detected using a high gain (G) amplifier (where loop
gain G is pre-settable in the model). The output of
the error amplifier is applied to the frequency
modulating (Fo) and pulsewidth control (PW) circuits.
The fixed frequency strategy chosen however needs to
be modified (Figure 4.23) to allow for restrictions in
minimum (Tmin) and maximum (Tmax) pulsewidths. Tmin is
the time required to allow for complete discharge of
snubber capacitor Cs prior to switching the transistor
off again. (T-Tmax) is the time required for the power
circuit to achieve steady state conditions following
transistor turn off. In the steady state situation

\[ \text{Pulsewidth (PW)} = \frac{(iL \cdot RL)}{VI \cdot Fo} \]
Schematic of control loop for the current source chopper

FIGURE 4.22

Pulse Width
Tmin

Tmax

--- V ---

loop current error

Pulse Width and Frequency control strategy

FIGURE 4.23

Simple thermal flow model for power device junction temperature calculation

FIGURE 4.24
As IL and RL vary, the control loop alters the pulsewidth such that

\[ T_{\text{min}} < \text{PW} < T_{\text{max}} \]

De-regulation of the output current results when PW > Tmax is demanded.

As shortcircuits (RL --> 0) are possible in the MIG process, equation (71) can produce values of PW --> 0.

In these circumstances, the pulsewidth is set at Tmin and the frequency is altered to maintain output regulation giving,

\[ \frac{i_L . RL}{VI} = T_{\text{min}} \times F_0 \quad \cdots \cdots (72) \]

Under transient conditions, the current error (\( \Delta i \)) dominates the determination of the pulsewidth such that if

\[ \Delta i > I_{\text{ref/G}}, \text{ then } \text{PW} = T_{\text{max}} \]

(ii) **Summary of additional equations used in the closed loop model**

The model was extended to predict the power loss in the active and passive devices. Using simplified thermal flow analysis (Figure 4.24), it was possible to estimate junction temperature attained in the power transistors and flywheel diodes.

\[ T_J = P_n \times R_{ja} + T_{amb} \quad \cdots \cdots (72) \]

where \( R_{ja} = \text{junction - ambient thermal resistance} \)

\[ P_n = \text{device power loss} \]
Power Dissipation Equations:

Transistor Power loss = \[ \sum_{n=1}^{N} iT(n) \times Uce(n) \] ....(74)

where \( N \) = Number of switching cycles

Flywheel diode loss = \( Qrr \times Vf \times F0 + \sum_{n=N}^{n=1} Uf(n) \times iF(n) \) ....(75)

Snubber circuit losses = \[ \sum_{n=1}^{N} IS(n) \times Rs \] ....(76)

Load Power (PLOAD) = \[ \sum_{n=1}^{N} iL(n) \times UL(n) \] ....(77)

An estimate of 2.5W/Ampere (PLOSS) of losses in other components in the welding machine has been made in order to predict system efficiency.

Total system loss (ZLOSS) = PLOSS+PTRAN+PDIODE+PSNUB

(iii) Response Time

The response of the chopper was predicted for a pulsed reference condition. The number of cycles required to attain the steady state condition was stored and converted into a rise time (tR) and fall time (tF).

(iv) Pre-set data limits

The initial running of the programme produced data that exceeded the limits specified for the power devices. The preset data of Figure 4.25 was therefore modified after each run in order to obtain results that did not exceed the maximum below: e.g. \( Lc \) was altered to reduce the transistor peak current if this exceeded 350A.
**Preset/Initial Conditions for Simulation Program**

```
001.00 =S  ; F/Diode recovery factor
000.22 =RZ  ; Zener resistance
000.10 =RS  ; Snubber discharge resistance
000.04 =RL  ; Load resistance
001.50 =UD  ; Diode forward volt drop
040.00 =VI  ; D.C. supply voltage
015.00 =VL  ; Load standing voltage
001.50 =UTR  ; Transistor saturation voltage
130.00 =VZ  ; Zener diode voltage
00.60E-06 =LC  ; Collector inductance
60.00E-06 =LF  ; Output inductance
01.50E-06 =LS  ; Snubber discharge inductance
00.20E-06 =LXE  ; Emitter stray inductance
00.20E-06 =LXF  ; F/Diode path stray inductance
00.20E-06 =LXS  ; Snubber capacitor stray inductance
04.00E-06 =CS  ; Snubber capacitance
1.500E-06 =TF  ; Transistor current fall time
00.250E-06 =TR  ; Transistor turn on time
10.00E-06 =QR  ; F/Diode recovered charge
00.00 =IC(1)  ; Initial value of IC
00.00 =IF(1)  ; Initial value of IF
00.00 =IL(1)  ; Initial value of IL
0.00 =IS(1)  ; Initial value of IS
0.00 =IT(1)  ; Initial value of IT
0.00 =IZ(1)  ; Initial value of IZ
60.00 =UCE(1)  ; Initial value of UCE
60.00 =US(1)  ; Initial value of US
15.00 =UL(1)  ; Initial value of UL
15.00E+03 =F  ; Frequency (F)
0250.0 =CIUREF  ; Peak current reference
100.0 =LING  ; Loop gain
000.10 =TRANSISTOR JUNCTION-CASE THERMAL RESISTANCE
000.10 =TRANSISTOR CASE-HEATSINK THERMAL RESISTANCE
000.05 =DIODE JUNCTION-CASE THERMAL RESISTANCE
000.07 =TRANSISTOR HEATSINK-AMBIENT THERMAL RESISTANCE
000.05 =DIODE CASE-HEATSINK THERMAL RESISTANCE
000.07 =DIODE HEATSINK-AMBIENT THERMAL RESISTANCE
025.00 =AMBIENT TEMPERATURE
003 =NTRAN
0050.0 =BACKGROUND CURRENT
END
```
Maximum Circuit Values

Peak Transistor Current (ITM) < 350A
Peak Transistor Voltage (UCEM) < 250V
Peak Flywheel Diode Current (IFM) < 400A
Maximum Transistor Junction Temperature (Tj) < 125 °C
Maximum Flywheel Diode Junction Temperature (TjD) < 150 °C
Supply Voltage Variation (Vi) 50-65V dc
Snubber Discharge Time (Tmin) < 5-7.5 us
Operating Frequency (Fo) > 15kHz
Maximum current rise (fall) time (tR,tF) < 0.5 ms
Maximum Output Ripple Current < 10A peak-peak
Maximum Load Current (iL) < 500A
Load Resistance Variation (RL) 5mA to 100mA

4.4.4 Closed Loop Performance and Results

Programme Description

The preset data for the closed loop model is given in Figure 4.25. All of the variables iL, iC, iT, iS are set to zero. The programme was run until the output current was within ± 2% of the reference (Iref). Similarly, it was assumed that initially the transistor was off and blocking the supply voltage (Vce = Vi) and that Cs was charged to Vi. The programme evaluates the equations every 250nS storing data at the end of each period of each cycle of operation. At the end of each cycle, the peak values attained by the variables are also stored. Figure 4.26 shows the data for a typical cycle in summarised form. The limiting factor in the amount of data that could be stored for
analysis, was the allocation of the computer memory to each user. For this reason, a maximum of 22 cycles of closed loop operation were possible. The circuit output would normally attain its steady state condition in less than this time (@ 100 us/cycle maximum).

The pre-set data was altered for each Iref to give results that were within the specification for the devices and the chopper circuit. The results for Iref from 200 to 375A are given in Appendix (A). These are summarised in Figure 4.27 where,

- the peak instantaneous values for ITM, IFM and UCEM occurring at any time during the 22 cycles are recorded
- device predicted temperatures, power dissipation etc are extracted from the final cycle (cycle 22)

The model results show that a transistor chopper operating at 15kHz and up to 250A of output current could be developed with the devices available. Higher output currents (up to 375A) could only be obtained with the use of higher current transistors and diodes. Such devices, with the required switching characteristics, are presently unavailable.

A 500A output could be achieved by paralleling two 250A rated Power Modules. Current sharing between the modules for dynamic and static loads needs to be ensured.

Results for the 250A Chopper

The chopper computer model was used to optimise the following circuit parameters (for Iref = 250A):

\[ V_i = \text{d.c. supply voltage}; \text{ an initial value of } 50V \text{ was chosen as a typical value for MIG welding} \]
A typical printout of data for the closed loop operation of the model

<table>
<thead>
<tr>
<th>J</th>
<th>XPD</th>
<th>KP</th>
<th>TK</th>
<th>ERR</th>
<th>ITM</th>
<th>IFM</th>
<th>IL[H]</th>
<th>USE[H]</th>
<th>USE[M]</th>
<th>IF[H]</th>
<th>IS[H]</th>
<th>ITM</th>
<th>UL</th>
<th>UCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>1</td>
<td>2145</td>
<td>0.40E+05</td>
<td>25.3</td>
<td>272.9</td>
<td>251.4</td>
<td>223.8</td>
<td>25.3</td>
<td>251.4</td>
<td>223.8</td>
<td>25.3</td>
<td>272.9</td>
<td>29.0</td>
<td>51.7</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>2146</td>
<td>0.42E-05</td>
<td>26.0</td>
<td>313.8</td>
<td>251.4</td>
<td>224.0</td>
<td>25.3</td>
<td>251.4</td>
<td>224.0</td>
<td>25.3</td>
<td>313.8</td>
<td>29.0</td>
<td>51.7</td>
</tr>
<tr>
<td>9</td>
<td>3</td>
<td>2147</td>
<td>0.45E-05</td>
<td>25.9</td>
<td>313.8</td>
<td>251.4</td>
<td>224.1</td>
<td>25.3</td>
<td>251.4</td>
<td>224.1</td>
<td>25.3</td>
<td>313.8</td>
<td>29.0</td>
<td>51.7</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>2341</td>
<td>0.53E-04</td>
<td>0.8</td>
<td>313.8</td>
<td>251.4</td>
<td>249.2</td>
<td>25.3</td>
<td>251.4</td>
<td>249.2</td>
<td>25.3</td>
<td>313.8</td>
<td>30.0</td>
<td>51.7</td>
</tr>
<tr>
<td>9</td>
<td>5</td>
<td>2350</td>
<td>0.55E-04</td>
<td>0.8</td>
<td>313.8</td>
<td>251.4</td>
<td>249.2</td>
<td>124.4</td>
<td>124.3</td>
<td>0.0</td>
<td>249.2</td>
<td>0.0</td>
<td>30.0</td>
<td>124.4</td>
</tr>
<tr>
<td>9</td>
<td>6</td>
<td>2351</td>
<td>0.56E-04</td>
<td>0.9</td>
<td>313.8</td>
<td>251.4</td>
<td>249.2</td>
<td>150.0</td>
<td>150.9</td>
<td>1.7</td>
<td>247.4</td>
<td>0.0</td>
<td>30.0</td>
<td>157.0</td>
</tr>
<tr>
<td>9</td>
<td>7</td>
<td>2358</td>
<td>0.57E-04</td>
<td>1.4</td>
<td>313.8</td>
<td>251.4</td>
<td>248.6</td>
<td>180.5</td>
<td>180.5</td>
<td>198.1</td>
<td>0.0</td>
<td>29.9</td>
<td>180.7</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td>2361</td>
<td>0.58E-04</td>
<td>1.6</td>
<td>313.8</td>
<td>251.4</td>
<td>248.4</td>
<td>180.5</td>
<td>180.5</td>
<td>248.4</td>
<td>0.0</td>
<td>29.9</td>
<td>180.7</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>2394</td>
<td>0.67E-04</td>
<td>3.8</td>
<td>313.8</td>
<td>371.9</td>
<td>246.2</td>
<td>51.0</td>
<td>51.0</td>
<td>275.9</td>
<td>-29.7</td>
<td>0.0</td>
<td>29.8</td>
<td>180.7</td>
</tr>
</tbody>
</table>

### Summary of Cycle 9 Data

- **J**: cycle number
- **KP**: data number
- **TK**: cycle time at period end
- **ERR**: current error
- **ITM**: peak transistor current during present cycle
- **IFM**: peak flywheel diode current during present cycle
- **IL[H]**, **UE[H]**, **IL[M]**, **UE[M]** are the load, f/diode, snubber and transistor currents respectively at the end of each period of the present cycle.
- **UL**: load voltage
- **UCM**: peak transistor voltage

---

**Figure 4.26**

---

### Summary of Cycle 10 Data

- **J**: cycle number
- **KP**: data number
- **TK**: cycle time at period end
- **ERR**: current error
- **ITM**: peak transistor current during present cycle
- **IFM**: peak flywheel diode current during present cycle
- **IL[H]**, **UE[H]**, **IL[M]**, **UE[M]** are the load, f/diode, snubber and transistor currents respectively at the end of each period of the present cycle.
- **UL**: load voltage
- **UCM**: peak transistor voltage

---

**Figure 4.26**
<table>
<thead>
<tr>
<th>$I_{ref}$ (kHz)</th>
<th>$F_o$ (µs)</th>
<th>$PW_t$ (µs)</th>
<th>ITM</th>
<th>IFM</th>
<th>UCEM</th>
<th>$t_{R-1F}$</th>
<th>$T_j$ (°C)</th>
<th>$T_jD$ (°C)</th>
<th>$PSNUB$ (W)</th>
<th>$PTRAN$ (W)</th>
<th>$PDIODE$ (W)</th>
<th>$Ntran$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>15</td>
<td>22</td>
<td>303</td>
<td>392</td>
<td>224</td>
<td>0.40</td>
<td>75.4</td>
<td>101</td>
<td>269</td>
<td>260</td>
<td>400</td>
<td>2</td>
</tr>
<tr>
<td>250</td>
<td>15</td>
<td>21</td>
<td>372</td>
<td>442</td>
<td>232</td>
<td>0.47</td>
<td>88.0</td>
<td>122</td>
<td>272</td>
<td>320</td>
<td>520</td>
<td>2</td>
</tr>
<tr>
<td>300</td>
<td>15</td>
<td>38</td>
<td>455</td>
<td>467</td>
<td>239</td>
<td>1.10</td>
<td>121.0</td>
<td>118</td>
<td>350</td>
<td>510</td>
<td>490</td>
<td>3</td>
</tr>
<tr>
<td>350</td>
<td>15</td>
<td>45</td>
<td>529</td>
<td>537</td>
<td>245</td>
<td>1.00</td>
<td>86.0</td>
<td>143</td>
<td>514</td>
<td>440</td>
<td>590</td>
<td>3</td>
</tr>
<tr>
<td>375</td>
<td>15</td>
<td>45</td>
<td>585</td>
<td>592</td>
<td>264</td>
<td>0.80</td>
<td>113.0</td>
<td>139</td>
<td>558</td>
<td>660</td>
<td>600</td>
<td>3</td>
</tr>
</tbody>
</table>

Device Limits: - - 350 400 250 2.00 125.0 150 - - -

*Model prediction of Performance for $I_{ref} = 200$ to 375A*

**FIGURE 4.27**
Fo = modulating frequency; an initial value of 15kHz was chosen, being the minimum frequency for inaudibility

Cs = snubber capacitance; a 5uF value was selected to limit the dv/dt across the main transistors to 50V/μs (Vi/Tf)

Tf = transistor fall time; with a value of 1μS

Lf = output filter inductance; 100uH was selected from arc stability considerations

Lc = collector inductance; 1 uH was chosen to limit transistor di/dt at turn on to 60A/μs

As each of these parameters was varied (e.g. Vi), the others were pre-set at their nominal values (e.g. Cs = 5 uF, Lc = 1 uH). The data obtained is given in Appendix (A) and are discussed below.

(i) Supply Voltage Vi Optimisation

The graphs of Figure 4.28a and 4.28b were plotted for a variation of Vi from 40 to 100V d.c..

Comments:

a) PDIODE + PTRAN = Constant (810 watts) for Vi > 40V.

b) The pulsewidth (transistor on time) decreases for increasing Vi as per equation (71). This reduces device saturation losses.

c) Ripple and transistor peak current increase linearly with Vi.

d) Lower values of pulse rise time (tR) are achieved with higher Vi values.

By imposing the specified limits of ripple current (10A) and maximum transistor current (350A), to
Figure 4.28a,b, a value of $V_1$ between 60 - 65V is determined as optimum. This corresponds to a value of $t_R$ of between 0.38 and 0.47 ms compared to the specified 0.5 ms. A value of $V_1 = 60V$ (@ 250A) is preferred in order to minimise transistor peak current levels.

(ii) Snubber Capacitance ($C_s$) Optimisation

The primary purpose of the snubber capacitor is to restrict the voltage across, and power dissipation in, the transistor to values permissible by the device SOAR. Residual circuit inductances store electrical energy $\frac{1}{2} L_1$ during the transistor on time. This is absorbed by the snubber capacitor $\frac{1}{2} C_s V_s$ after $T_R$ turns off.

From the $U_{ce} x C_s$ plot of Figure 4.29, $C_s$ can be selected to ensure that the $V_{cex}$ rating of the transistors are not exceeded.

For the ESM 3001 ($V_{cex} = 200$) and DT63 ($V_{cex} = 350V$) $C_s$ values of 3.9uF and 1.9uF respectively are predicted.

The energy stored in the snubber capacitor is dissipated in the snubber resistance ($R_s$) and $T_R$.

This loss is shown to have an exponential form for $C_s < 4$ uF and is linear for $C_s > 5$ uF. A minimum is observed to occur at $4 \pm 0.2$ uF. The very high losses for low values of $C_s$ are due to the high capacitor voltage attained in absorbing the inductive energy from $L_c$ and stray inductance. The losses vary according to the dissipation equation

$$P_s = \frac{1}{2} C_s U_{ce} \times F_0$$

suggesting that $U_{ce}$ should be minimised to reduce $P_s$. 
Effect of varying snubber capacitance $C_s$

**FIGURE 4.29**

- $P_{snub}$ - snubber circuit losses
- Optimum value, 4.0uF
- $V_{out}$ - transistor voltage - $U_{ce}$

![Graph showing the effect of varying snubber capacitance on $P_{snub}$ and $U_{ce}$](image-url)
For high values of $C_s$, $U_{ce}$ is at an almost constant level and the loss is then determined by $C_s$ only - hence its linear form in Figure 4.29. The optimum snubber value is 4.0uF, giving a dissipation of 290W and a $U_{ce}$ value of 190V, the latter being within the rating of the transistors selected.

(iii) Modulating Frequency - $F_o$

The variation of response time ($t_R$, $t_F$), TR power dissipation ($P_{TRAN}$) and load ripple current with $F_o$ are plotted in Figure 4.30. As expected, there is an increase in transistor losses with an increase in $F_o$ (5W/kHz). The ripple current (for $L_f = 60$ uH) decreases linearly at approximately 1A/kHz.

Applying the chopper specification to Figure 4.30, for a ripple current of 10A, $F_o = 15.6$kHz. Other considerations in determining the frequency of operation are:
- maximum permissible junction temperature for the power transistor and flywheel diode
- limit of audibility (> 15kHz)

(iv) Output Inductance - $L_f$

The output inductor serves to smooth the output current and store energy to counteract fast changes in the arc impedance. The two factors which determine the choice of $L_f$ values are response time and load current ripple amplitude. The minimum value of $L_f$ is set at 25 uH from arc stability criteria. From Figure 4.31, the rise time is seen to vary linearly with output inductance. To restrict $t_R$ to a
Effect of varying $P_o$

Transistor power loss - watts

Load ripple current amplitude

$P_{tran}$

10A, 15.6 kHz

FIGURE 4.30
value less than 0.5 mS, Lf cannot exceed 60 uH. The ripple current however, varies non-linearly. At the specified ripple of 10A, Lf = 60uH. 60uH was selected giving values of tR = 0.47 mS and Δi = 10A.

(v) Transistor Fall time - Tf

For operation at high frequencies (> 10kHz) and currents (> 350A), the transistor must have fast turn on and turn off times. The device current fall time (Tf) determines the snubber capacitance required and the switching losses in the transistor.

From Figure 4.32a,b, for a given value of Cs, the voltage across the transistor increases rapidly for Tf values greater than 1.75μs. A significant decrease in Vce is observed for Tf < 0.5μs. This occurs because the charge (Q = Cs.Vce) equals the area of the iT x time waveform. The longer the fall time, the higher the value of Vce. Transistor fall times < 1 μs are therefore preferred in order to restrict snubber circuit losses and device Vce. Higher Vce levels also increase the current in Df (due to higher iS currents in the resonants charge/discharge cycles) and results in increased snubber circuit losses (Figure 4.32a).

The switching losses in the transistor increase @ 35W/μs for Tf values above 0.5 μs.

(vi) Collector Inductance - Lc

When the transistor turns on, the flywheel diode is immediately reverse biased and goes into its recovery mode. The diode reverse recovery current is conducted
Effect of varying output inductance $L_f$

$t_R = \text{rise time of load current 0-100}\% I_{ref}$

- Rise time $t_R$:
  - $0.47\text{ms}, 60\mu\text{H}$
  - $60\mu\text{H}, 10\text{A}$

FIGURE 4.31
by the transistor and the peak current demand on the transistor occurs at this time (Figure 4.16). The collector inductance $L_c$ helps to limit the diode recovery current and hence transistor peak current $I_{TM}$. As shown in Figure 4.33, $I_{TM}$ can be reduced by 50A by using a 1 uH inductance rather than depending on stray cable inductance (0.2uH). The disadvantage in the use of $L_c$ is that the energy stored in $L_c$ is absorbed by $C_S$ during turn-off causing an increase in $U_{CE}$. A value of 0.5uH was therefore chosen as a compromise.

(vii) Optimised values for circuit constants
The optimised values for the circuit constants from the preceding sections are:

\[
\begin{align*}
V_i &= 60V \\
C_s &= 4.0uF \\
T_f &< 1.0uS \\
L_f &= 60uH \\
L_c &= 0.5uH \\
F_o &= 15kHz
\end{align*}
\]

(viii) Continuous Current Operation
Using the optimised values for circuit parameters from above, the programme was run to simulate operation under typical arc loads conditions:
- normal arc $RL = 0.04\Omega$, $VL = 15$ to 20V
- short circuit arc $RL = 0.04\Omega$, $VL = 0.1V$
These result are given in Appendix (A). A summary of the results is given in Figure 4.35a,b. These indicate
Effect of varying collector circuit inductance $L_c$

**FIGURE 4.33**

- Peak diode current
- Peak transistor current
- Transistor collector-emitter voltage $U_{ce}$

Current - Amperes

Voltage - volts

Inductance - $\mu$H
<table>
<thead>
<tr>
<th>Optimised Value</th>
<th>IFM (A)</th>
<th>ITM (A)</th>
<th>Vce (V)</th>
<th>AI (A)</th>
<th>tR (W)</th>
<th>PTRAN (W)</th>
<th>PSNUB (W)</th>
<th>PDIODE (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1=60</td>
<td>385</td>
<td>343</td>
<td>194</td>
<td>9.6</td>
<td>0.47</td>
<td>280.0</td>
<td>-</td>
<td>525</td>
</tr>
<tr>
<td>Lf=60uH</td>
<td>393</td>
<td>359</td>
<td>194</td>
<td>10.0</td>
<td>0.47</td>
<td>280.0</td>
<td>-</td>
<td>530</td>
</tr>
<tr>
<td>Cm=4uF</td>
<td>384</td>
<td>359</td>
<td>190</td>
<td>-</td>
<td>0.47</td>
<td>280.0</td>
<td>270</td>
<td>530</td>
</tr>
<tr>
<td>Fo=15.75kHz</td>
<td>393</td>
<td>359</td>
<td>194</td>
<td>10.0</td>
<td>0.46</td>
<td>287.5</td>
<td>-</td>
<td>530</td>
</tr>
<tr>
<td>Tt=1μs</td>
<td>383</td>
<td>334</td>
<td>174</td>
<td>-</td>
<td>0.47</td>
<td>250.0</td>
<td>220</td>
<td>530</td>
</tr>
<tr>
<td>Lc=0.6uH</td>
<td>383</td>
<td>354</td>
<td>195</td>
<td>10.0</td>
<td>0.47</td>
<td>290.0</td>
<td>-</td>
<td>530</td>
</tr>
</tbody>
</table>

**SPECIFICATION:**

| 400  | 350  | 250  | 5A   | 0.5  | -    | -       | -       |

*Optimised data x Performance*

*Figure 4.34*
<table>
<thead>
<tr>
<th>Iref (kHz)</th>
<th>Fo (µs)</th>
<th>PW (us)</th>
<th>ITM</th>
<th>IFM</th>
<th>UCEM</th>
<th>VL/IL</th>
<th>tR (ms)</th>
<th>Tj (°C)</th>
<th>Tjd (°C)</th>
<th>PSNURB (W)</th>
<th>PTRAN (W)</th>
<th>PDIODE (W)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>175</td>
<td>15</td>
<td>17</td>
<td>273</td>
<td>275</td>
<td>154</td>
<td>21.8</td>
<td>170.0</td>
<td>0.27</td>
<td>56.3</td>
<td>95</td>
<td>-</td>
<td>150</td>
<td>330</td>
</tr>
<tr>
<td>200</td>
<td>15</td>
<td>20</td>
<td>284</td>
<td>309</td>
<td>160</td>
<td>22.9</td>
<td>197.3</td>
<td>0.40</td>
<td>65.0</td>
<td>102</td>
<td>-</td>
<td>190</td>
<td>370</td>
</tr>
<tr>
<td>250</td>
<td>15</td>
<td>30</td>
<td>343</td>
<td>384</td>
<td>185</td>
<td>29.8</td>
<td>245.5</td>
<td>-</td>
<td>91.0</td>
<td>123</td>
<td>-</td>
<td>330</td>
<td>480</td>
</tr>
</tbody>
</table>

RL = 0.04 Ω  
VL = 15.0V

Summary of results into a normal arc load

FIGURE 4.35a

<table>
<thead>
<tr>
<th>Iref (kHz)</th>
<th>Fo (µs)</th>
<th>PW (us)</th>
<th>ITM</th>
<th>IFM</th>
<th>UCEM</th>
<th>VL/IL</th>
<th>tR (ms)</th>
<th>Tj (°C)</th>
<th>Tjd (°C)</th>
<th>PSNURB (W)</th>
<th>PTRAN (W)</th>
<th>PDIODE (W)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>4.3</td>
<td>3.2</td>
<td>116</td>
<td>62</td>
<td>66</td>
<td>1.34/49.6</td>
<td>0.58</td>
<td>27.0</td>
<td>32.0</td>
<td>-</td>
<td>6.7</td>
<td>30</td>
<td>12.8</td>
</tr>
<tr>
<td>100</td>
<td>9.7</td>
<td>6.2</td>
<td>174</td>
<td>144</td>
<td>108</td>
<td>2.56/98.3</td>
<td>0.68</td>
<td>31.3</td>
<td>57.4</td>
<td>-</td>
<td>23.0</td>
<td>160</td>
<td>31.2</td>
</tr>
<tr>
<td>150</td>
<td>15.0</td>
<td>6.2</td>
<td>233</td>
<td>236</td>
<td>141</td>
<td>3.74/145.8</td>
<td>0.13</td>
<td>39.0</td>
<td>89.0</td>
<td>-</td>
<td>55.0</td>
<td>320</td>
<td>38.1</td>
</tr>
<tr>
<td>175</td>
<td>15.0</td>
<td>7.2</td>
<td>258</td>
<td>272</td>
<td>153</td>
<td>4.33/169.1</td>
<td>0.60</td>
<td>43.0</td>
<td>104.0</td>
<td>-</td>
<td>73.0</td>
<td>390</td>
<td>40.7</td>
</tr>
<tr>
<td>200</td>
<td>15.0</td>
<td>7.2</td>
<td>285</td>
<td>310</td>
<td>166</td>
<td>4.95/193.8</td>
<td>0.20</td>
<td>47.0</td>
<td>121.0</td>
<td>-</td>
<td>88.0</td>
<td>470</td>
<td>43.2</td>
</tr>
<tr>
<td>225</td>
<td>15.0</td>
<td>9.0</td>
<td>315</td>
<td>343</td>
<td>176</td>
<td>5.54/217.5</td>
<td>0.60</td>
<td>54.0</td>
<td>135.0</td>
<td>-</td>
<td>120.0</td>
<td>540</td>
<td>45.3</td>
</tr>
<tr>
<td>250</td>
<td>15.0</td>
<td>9.2</td>
<td>330</td>
<td>381</td>
<td>187</td>
<td>6.16/242.6</td>
<td>0.40</td>
<td>59.0</td>
<td>154.0</td>
<td>-</td>
<td>150.0</td>
<td>640</td>
<td>47.2</td>
</tr>
</tbody>
</table>

RL = 0.025 Ω  
VL = 0.1V

Summary of results into a shortcircuit arc load

FIGURE 4.35b
that operation at up to 200A (Iref) is achievable without exceeding the limits imposed on the ratings of the semiconductors. At Iref = 250A, the junction temperature (TjD) of Df exceeds the maximum specified. Higher device and circuit currents, voltages and power dissipation levels are also observed. These are not in proportion with the change in Iref from 200 to 250A. In the shortcircuit mode, the transistor is in conduction for between 3 - 9 μs in each cycle. Df conducts the load current for the remainder of the cycle. This represents the worst case operating condition for Df during which time, the device is seen to attain a junction temperature close to its maximum. The general conclusion drawn is that the Power Module could be operated at up to 200A (Iref) continuous. 250A operation would be possible only with some form of thermal duty cycling.

(ix) Pulse Response Time

The dynamic performance of the model was evaluated by switching the current reference between 2 levels representing pulsed peak (Ip) and background (Ib) currents. Figure 4.36 is a print out of data obtained for Ip = 200, Ib = 25A. Rise times (tR) of 0.4 and fall times (tF) of 1.3 ms are predicted for a constant arc resistance of 0.04Ω. In practice, faster fall times are envisaged as the arc resistance increases with a decrease in arc current. This is predicted by the arc simulation results of Figure 4.38.
Computer model prediction of power module response to a pulsed reference

- $E_m = 0.04R$
- $V_L = 15V$
- $I_p = 200A$
- $I_b = 25A$

**Figure 4.26**
which shows that as RL is varied between 0.01 and 0.12 ohms, tF decreases. The resistance of the arc can vary between the minimum (< 10 mS) and open circuit (1Kohm) in less than 100 uS. If the resistance is greater than the maximum allowable, de-regulation of the output occurs (Figure 4.37, RL=0.4Ω). In the extreme case, the arc extinguishes. It can therefore be concluded that the performance of a constant current characteristic power source can be influenced by external factors that alter the impedance of the arc (e.g. changes in torch - workpiece separation, magnetic effects etc).

Pulsing Iref between Ip (200A) and Ib (for values of 25, 50 and 100A respectively) produces waveforms shown in Figure 4.39. It can be seen that the shape of the initial portion of the fall is almost identical, higher background level producing shorter fall times.

The theoretical maximum bandwidth (Fp) of the Power Module is given by

\[ Fp = \frac{1}{(tR + tF)} \]

Using data from Figure 4.36, (tR = 0.4mS; tF = 1.3mS) gives Fp = 588.23 Hz.

4.5 Summary of data obtained from the computer Model of the Transistor Chopper

The device ratings and output performance obtained for Iref = 250A operation into a normal arc load are given in Figure 4.40.
Load current regulation for varying load resistances (RL)

For Iref = 175A

<table>
<thead>
<tr>
<th>J</th>
<th>0.15E+09</th>
<th>0.35E+09</th>
<th>0.55E+09</th>
<th>0.75E+09</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74.75</td>
<td>39.38</td>
<td>36.86</td>
<td>18.80</td>
</tr>
<tr>
<td>2</td>
<td>85.86</td>
<td>79.52</td>
<td>67.05</td>
<td>27.16</td>
</tr>
<tr>
<td>3</td>
<td>145.14</td>
<td>144.33</td>
<td>100.50</td>
<td>25.17</td>
</tr>
<tr>
<td>4</td>
<td>192.72</td>
<td>197.91</td>
<td>126.23</td>
<td>27.85</td>
</tr>
<tr>
<td>5</td>
<td>229.49</td>
<td>241.78</td>
<td>145.75</td>
<td>30.23</td>
</tr>
<tr>
<td>6</td>
<td>251.97</td>
<td>271.55</td>
<td>154.18</td>
<td>32.39</td>
</tr>
<tr>
<td>7</td>
<td>263.01</td>
<td>273.10</td>
<td>152.53</td>
<td>33.36</td>
</tr>
<tr>
<td>8</td>
<td>254.06</td>
<td>275.89</td>
<td>152.20</td>
<td>32.01</td>
</tr>
<tr>
<td>9</td>
<td>273.20</td>
<td>275.99</td>
<td>156.27</td>
<td>31.74</td>
</tr>
<tr>
<td>10</td>
<td>273.20</td>
<td>275.99</td>
<td>156.22</td>
<td>31.80</td>
</tr>
<tr>
<td>11</td>
<td>273.20</td>
<td>275.99</td>
<td>156.20</td>
<td>31.80</td>
</tr>
<tr>
<td>12</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>13</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>14</td>
<td>273.21</td>
<td>275.97</td>
<td>156.25</td>
<td>31.84</td>
</tr>
<tr>
<td>15</td>
<td>273.21</td>
<td>275.96</td>
<td>156.26</td>
<td>31.84</td>
</tr>
</tbody>
</table>

For Iref = 175A

<table>
<thead>
<tr>
<th>J</th>
<th>0.15E+09</th>
<th>0.35E+09</th>
<th>0.55E+09</th>
<th>0.75E+09</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74.75</td>
<td>39.38</td>
<td>36.86</td>
<td>18.80</td>
</tr>
<tr>
<td>2</td>
<td>85.86</td>
<td>79.52</td>
<td>67.05</td>
<td>27.16</td>
</tr>
<tr>
<td>3</td>
<td>145.14</td>
<td>144.33</td>
<td>100.50</td>
<td>25.17</td>
</tr>
<tr>
<td>4</td>
<td>192.72</td>
<td>197.91</td>
<td>126.23</td>
<td>27.85</td>
</tr>
<tr>
<td>5</td>
<td>229.49</td>
<td>241.78</td>
<td>145.75</td>
<td>30.23</td>
</tr>
<tr>
<td>6</td>
<td>251.97</td>
<td>271.55</td>
<td>154.18</td>
<td>32.39</td>
</tr>
<tr>
<td>7</td>
<td>263.01</td>
<td>273.10</td>
<td>152.53</td>
<td>33.36</td>
</tr>
<tr>
<td>8</td>
<td>254.06</td>
<td>275.89</td>
<td>152.20</td>
<td>32.01</td>
</tr>
<tr>
<td>9</td>
<td>273.20</td>
<td>275.99</td>
<td>156.27</td>
<td>31.74</td>
</tr>
<tr>
<td>10</td>
<td>273.20</td>
<td>275.99</td>
<td>156.22</td>
<td>31.80</td>
</tr>
<tr>
<td>11</td>
<td>273.20</td>
<td>275.99</td>
<td>156.20</td>
<td>31.80</td>
</tr>
<tr>
<td>12</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>13</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>14</td>
<td>273.21</td>
<td>275.97</td>
<td>156.25</td>
<td>31.84</td>
</tr>
<tr>
<td>15</td>
<td>273.21</td>
<td>275.96</td>
<td>156.26</td>
<td>31.84</td>
</tr>
</tbody>
</table>

For Iref = 175A

<table>
<thead>
<tr>
<th>J</th>
<th>0.15E+09</th>
<th>0.35E+09</th>
<th>0.55E+09</th>
<th>0.75E+09</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74.75</td>
<td>39.38</td>
<td>36.86</td>
<td>18.80</td>
</tr>
<tr>
<td>2</td>
<td>85.86</td>
<td>79.52</td>
<td>67.05</td>
<td>27.16</td>
</tr>
<tr>
<td>3</td>
<td>145.14</td>
<td>144.33</td>
<td>100.50</td>
<td>25.17</td>
</tr>
<tr>
<td>4</td>
<td>192.72</td>
<td>197.91</td>
<td>126.23</td>
<td>27.85</td>
</tr>
<tr>
<td>5</td>
<td>229.49</td>
<td>241.78</td>
<td>145.75</td>
<td>30.23</td>
</tr>
<tr>
<td>6</td>
<td>251.97</td>
<td>271.55</td>
<td>154.18</td>
<td>32.39</td>
</tr>
<tr>
<td>7</td>
<td>263.01</td>
<td>273.10</td>
<td>152.53</td>
<td>33.36</td>
</tr>
<tr>
<td>8</td>
<td>254.06</td>
<td>275.89</td>
<td>152.20</td>
<td>32.01</td>
</tr>
<tr>
<td>9</td>
<td>273.20</td>
<td>275.99</td>
<td>156.27</td>
<td>31.74</td>
</tr>
<tr>
<td>10</td>
<td>273.20</td>
<td>275.99</td>
<td>156.22</td>
<td>31.80</td>
</tr>
<tr>
<td>11</td>
<td>273.20</td>
<td>275.99</td>
<td>156.20</td>
<td>31.80</td>
</tr>
<tr>
<td>12</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>13</td>
<td>273.21</td>
<td>275.93</td>
<td>156.23</td>
<td>31.86</td>
</tr>
<tr>
<td>14</td>
<td>273.21</td>
<td>275.97</td>
<td>156.25</td>
<td>31.84</td>
</tr>
<tr>
<td>15</td>
<td>273.21</td>
<td>275.96</td>
<td>156.26</td>
<td>31.84</td>
</tr>
</tbody>
</table>

FIGURE 4.37
Effect of RL on $t_R, t_F$ during pulsed current operation

FIGURE 4.38

$t_R, t_F$ under pulsed load current conditions and varying background currents

FIGURE 4.39
### Flywheel Diode (Df)

- **IFM (peak)**: > 384A
- **Qrr**: < 10 μC
- **S**: > 1 (recovery softness factor)
- **Vf**: < 1.5V @ 400A
- **Rj-c**: < 0.05 C/watt
- **PDIODE**: > 640W

### Main Transistor (TR)

- **ITM**: > 343A
- **Vce**: > 187V
- **PTRAN**: > 330W
- **Tf**: < 1us
- **Rj-c**: < 0.08 C/W
- **Vce(sat)**: < 1.5V

### Inductances

- Interconnecting cable inductance < 0.2uH

### Output Performance

- **Current Ripple**: < 10A
- **Pulse Rise Time (tR)**: < 0.4ms
- **Pulse Fall Time**: < 1.13ms
- **Power bandwidth (Hz)**: < 588.23Hz
- **Efficiency (%) @ 200A**: 78.3, RL = 0.04
- **@ 250A**: 82.0, VL = 15.0V

### Summary of data obtained from Model of Transistor Chopper @ 250A = Iref

Figure 4.40
5. DESIGN OF A 250 AMPERE, 15kHz TRANSISTOR CHOPPER

5.0 Introduction

The chopper circuit of Figure 5.1 shows the optimised values of circuit components and power semiconductor requirements based on the computer model results of Chapter 4. The electrical properties of the semiconductors used are discussed with a view to producing a practical design of the transistorised chopper.

5.1 Choice of Power Transistors

5.1.1 Power Transistor Characteristics

Collector-Emitter Sustaining Voltage

The avalanche characteristics of a typical triple diffused transistor is given in Figure 5.2. The curves define the Vce blocking capability of the device under different base-emitter bias conditions:

- \( V_{cer} \) for a low resistance across the base-emitter (\( R_{be} \))
- \( V_{cex} \) for a negative Vbe bias (-Vbe)
- \( V_{ceo} \) for no -Vbe or Rbe

From Figure 4.40, the required Vce rating of the transistor needs to be a minimum of 187 Volts.

On-state collector-emitter voltage [Vce(sat)]

Triple diffused transistors are able to withstand high voltages because of the inclusion of a high resistivity N- region in their construction - Figure 5.3. When the device is forward biased with an injection of base current, minority carrier charges cause an extension of the P- type base region into the N- collector region.
Power module circuit showing optimised component values

FIGURE 5.1
Collector-emitter avalanche characteristics of a transistor as a function of emitter-base drive. We can see that the open base collector-emitter avalanche characteristic $V_{CEO}$ is always the lowest in voltage. This characteristic exhibits a vertical zone which corresponds to the lowest value of collector-emitter voltage. This value is called $V_{CEO(sus)}$ and is guaranteed by the manufacturer.

Structure of an NPN triple diffused power transistor
effectively reducing the collector resistance.
The collector current is maintained by injection of additional charges from the base circuit. The saturation voltage of the device is therefore the product of collector current and resistance. Additional base current will cause the virtual base region to extend into the N+ region - full saturation of the device being attained when the collector region resistance is at its minimum and cannot be further reduced by charge modulation. To achieve $V_{ce(sat)}$ status, the base current must be capable of supporting the collector current and the fully modulated state of the device.

**Device Switching Times** (Figure 5.4a,b)
The switching performance of a triple diffused device is dependent on the level (and control) of minority carrier charges in the base and collector regions during the turn-on and turn-off periods.

**Turn-on Time $T_d$, $T_r$**
When the base-emitter is forward biased, there is a short delay ($T_d$) before collector current flows. This occurs for two reasons:

a) the initial high resistance of the base region prevents the flow of base current

b) the base-emitter junction capacitance ($C_{be}$) diverts base current from the junction until it is fully charged

$T_d$ values are not quoted by manufacturers but are estimated at < 0.25 μS.
The voltage across the device reduces under the influence of the base current. Initially, the device goes into a period of dynamic saturation prior to settling at a lower level of saturation voltage. The total delay (Tr) to saturation is dependent on circuit conditions and the base drive characteristics.

**Turn-off Times . . . Ts, Tf**

To return the transistor to its blocking state, the injection of charges needs to be stopped and the charges stored in the device removed in a controlled manner. Negative base-emitter bias produces a flow of reverse base current which removes the stored charges. Initially, (Figure 5.4b, period Ts) there is no perceptible change in collector current which is sustained by surplus charges. The collector current then reduces rapidly to zero and the device Vce rises as the N- collector region recovers to its high resistance mode. The device operates in the linear mode during the fall time period and as such the d(Ic)/dt is controlled by d(Ib)/dt. This is a period of high dissipation and optimisation of the fall time is essential. As shown in Figure 5.4c, this is achieved by allowing the collector-base and base-emitter junctions to recover their blocking states together. If the base-emitter junction recovers first, transistor action is lost and the collector-base junction recovery behaviour is similar to that of a diode. This produces a tail of current at the end of the fall time, under high Vce conditions.
Collector

Base

Emitter

Simplified representation of the internal impedances of a power transistor

FIGURE 5.4a

Transistor switching waveforms used to define switching times

FIGURE 5.4b
Possible turn-off modes of a transistor: evolution of base-emitter and collector base junction.

A: base-emitter junction cut-off last: progressive desaturation of the transistor, leading to a tail at the onset of the fall time of the collector current: high losses.

B: base-emitter junction cut-off first: recovery of a large part of the collector base capacitance charge, tail at the end of the fall time of collector current decrease: high losses.

C: junctions cut-off simultaneously: minimal losses.

FIGURE 5.4c

Different switching phases of the transistor:

a and f: cut-off state
b: variation of base-emitter capacitance charge. the junction is forward biased, the transistor is at the conduction threshold
c: rise of collector current: movement of the virtual junction in the collector zone, accumulation of neutralising charges in the collector, accumulation of charges in the total base region linked to the final value of collector current.
d: elimination of superfluous charges: neither modification to collector current nor to saturation voltage \( V_C(E_{Sat}) \)
e: progressive elimination of all the charges: reduction of collector current, return to cut-off of base-emitter and collector base junctions independently one from the other.

FIGURE 5.4d
If the collector-base junction recovers first, the device de-saturates progressively and the collector current waveform droops at the start of the fall time which produces high dissipation in the transistor. The evolution of turn on and turn off mechanisms in the transistor are illustrated in Figure 5.4d.

Collector current ratings $I_c(sat), I_{CM}$

The $I_c(sat)$ rating is defined as the maximum current the device will conduct and still be guaranteed to be in saturation [$V_{ce(sat)}$] under forced gain conditions. Higher currents, up to the $I_{CM}$ level, are possible but the device voltage saturation level cannot be guaranteed and will always be greater than $V_{ce(sat)}$.

From Figure 4.40, for 250A operation, the model predicts peak currents up to 343A. Neither the ESM3001 [$I_c(sat) = 150A; I_{CM} = 300A$] or the DT63 [$I_c(sat) = 250A; I_{CM} = 450A$] are capable of conducting the required 343A. It would therefore be necessary to operate multiple devices in parallel.

Safe Operating Area (SOAR)

SOAR ratings of transistors represent the maximum, simultaneous limits of current and voltage that the device is permitted (for a given junction temperature). Operation outside these limits could result in immediate failure or degradation in device characteristics. SOAR curves are published for forward and reverse biased operation of the base-emitter junction.
The base-emitter junction is not uniformly biased due to the distributed resistance of the base region (Figure 5.5a). Consequently, in the forward biased mode (Vbe > 0), the centre of the emitter structure is least forward biased and current concentration occurs in the periphery of the emitter (Figure 5.5a). The resulting concentration of energy (Vce.Ic.Tr) can cause "hot spots" to develop along the emitter periphery, leading to device failure. This energy limit is defined by the forward biased SOAR.

In the reverse bias mode (Vbe < 0), the distributed base resistance leaves the centre of the emitter region slightly forward biased and the peripheral emitter regions cut-off (Figure 5.5b). The current flow in the device during the storage and fall time periods therefore occurs at the emitter centre. The permitted energy concentration [Vce.Ic.(Ts+Tf)] is limited by the reverse biased SOAR.

5.1.2 Parallel Operation of Transistors

The static and dynamic sharing of current in a parallel group of transistors is influenced by:

- the spread in device characteristics (Vbe(sat), Vce(sat), Ts etc)
- asymmetry in the wiring of the devices to the base drive circuit, collector supply, load etc

A number of authors have examined the problem of current sharing in high current (> 100A) triple diffused transistors. Current sharing during
The voltage $V_{BE}$ applied to the base-emitter junction reduces as the center of the emitter is approached because of the distributed base resistance $r$: $V_{\text{junction}} = V_{BE} = \Sigma I_{Bj}$. The current density is a maximum at the emitter periphery. At high currents, this density limits the voltage rating of the collector base junction at point A for a given conduction time.

**FIGURE 5.5a**

*THE TRANSISTOR FORWARD BIASED: DEFOCUSING PHENOMENON*

The reverse voltage $V_{BB}$ applied to the base-emitter reduces in amplitude as we move away from the emitter periphery because of the distributed base resistance $r$: $V_{\text{junction}} = |V_{BB}| - V_{BE} = |\Sigma I_{Bj}|$. The outside of the emitter is cut-off, but the center remains in conduction. The resultant current density can limit, even during the very short time corresponding to the fall time $t_f$ of the collector current, the voltage rating of the collector base junction of the transistor.

**FIGURE 5.5b**

*THE TRANSISTOR REVERSE BIASED*
the saturated states and under switching conditions are influenced in different ways.

Current sharing during the saturated and quasi-saturated states

Devices operating in quasi-saturation (e.g. Darlington configuration) need to have their Vbe(sat) matched to within:
- 0.15V for a ± 20% mismatch (mismatch measured relative to nominal current for each device)
- 0.025V for a ± 5% mismatch
- unmatched for ± 50% mismatch

This assumes that the base-emitter and collector terminals of all the devices are directly coupled, that the interconnecting resistances and inductances are equal and that the circuit layout around the devices is symmetrical.

In the saturated state, the resistance of the collector-emitters [Rce(sat)] determines the sharing. In both modes, addition of resistances (> 3 mΩ) into each emitter will ensure current sharing to within ± 20% of the nominal level.

In all cases, the design criteria is to ensure that no device in the parallel stack exceeds its Ic(sat), power dissipation or SOAR ratings at any time during the switching cycle.

Current sharing in the switching states

The level of stored charges in the devices vary, giving rise to different storage times (Ts) for the devices. Those with the longest Ts will conduct the
full load current just prior to their fall time period. However, by applying a reverse bias to the base-emitter junctions, it has been shown that the charge removal is usually impaired in the transistors with a short $T_s$ value and enhanced in those with a longer $T_s$. The result is that the devices switch off together. Storage times need to be matched to within 0.5μs (at nominal device current). Symmetrical wiring is also necessary. The base-emitter junction of the devices need to be directly coupled for the above auto-sharing process to work.

Calculation of the number of devices in Parallel

From Figure 4.40, the maximum current conducted by the transistors is 343A for a 250A load current. The worst case design is for the use of unmatched devices - this is a practical proposition on the grounds of costs, field servicing etc.

a) If 2 devices (TA, TB) are connected in parallel, assume that one device (TA) passes 50% of its nominal current.

\[
\begin{align*}
    \text{ITA} &= 171.5 \times 0.5 = 85.75A \\
    \text{ITB} &= 343 - 85.75 = 260.5
\end{align*}
\]

b) If 3 devices (TA, TB, TC) are connected in parallel, and assuming that one device (TA) conducts the minimum current and another (TB) the maximum (+50%),

\[
\begin{align*}
    \text{ITA} &= 114.3 \times 0.5 = 57.2A \\
    \text{ITB} &= 114.3 \times 1.5 = 171.45 \\
    \text{ITC} &= 343 - 57.2 -171.45 = 114.35
\end{align*}
\]
The ESM3001 could be used under condition (b) only, although the current in one of the group of three is greater than 150A. The DT63 device could be used for both conditions.

5.1.3 Transistor Darlington Operation

The use of transistors to control high currents (> 100A) necessitates the use of the Darlington configuration in order to minimise the base current requirements.

The principal advantage of the Darlington transistor is its high current gain. A single stage Darlington composed of discrete devices is shown in Figure 5.6a. R1 and R2 provide a path for the leakage currents of the driver device (T1) and the output device (T2) when the Darlington is in the blocking state. The overall gain is given as

\[ g_{\text{out}} = g_{1} + g_{1.2} + 2 \left(1 - V_{\text{BE2}} \right) \frac{R_{1}}{R_{2} I_{B1}} \]  \( \text{(80)} \)

which is approximated to

\[ g_{\text{out}} = g_{1.2} \]  \( \text{(81)} \)

Using data from Appendix B for the ESM3001 (DT63), and that for a typical driver device (TC40U), a forward bias base current of 1.22A (4.10A) and a reverse bias current of 24.39A (41.05A) peak are required to switch the Darlington under worst case conditions - Figure 5.7, (Figure 5.8).

One of the principal disadvantages of the Darlington is the increase in the on state saturation voltage.

Under forced gain conditions,

\[ V_{\text{ce(sat)}} = V_{\text{ce(sat)}} + V_{\text{be(sat)}} \]  \( \text{(82)} \)
Darlington switch waveforms at turn on

FIGURE 5.6a

Darlington switch waveforms at turn off

FIGURE 5.6b
Data for Darlington Configuration using ESM3001 Devices

FIGURE 5.7

<table>
<thead>
<tr>
<th>TA</th>
<th>TB</th>
<th>TC</th>
<th>T1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ic</td>
<td>57.20</td>
<td>171.45</td>
<td>114.35</td>
</tr>
<tr>
<td>hfe(min) @ Ic</td>
<td>37.50</td>
<td>10.00</td>
<td>20.00</td>
</tr>
<tr>
<td>Ib = Ic/hfe(min)</td>
<td>1.52</td>
<td>17.15</td>
<td>5.72</td>
</tr>
<tr>
<td>Vbe @ Ic</td>
<td>1.00</td>
<td>1.45</td>
<td>0.55</td>
</tr>
<tr>
<td>Vce(sat) @ Ic</td>
<td>0.20</td>
<td>1.30</td>
<td>1.25</td>
</tr>
</tbody>
</table>

(* Ic of T1) = 1.52 + 17.15 + 5.72)

Vce(sat)2 = 1.25 + 0.55 = 1.8 (min)

1.25 + 1.45 = 2.7 (max)

Data for Darlington Configuration using DT63 Devices

FIGURE 5.8

<table>
<thead>
<tr>
<th>TA</th>
<th>TB</th>
<th>T1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ic</td>
<td>85.75</td>
<td>257.25</td>
</tr>
<tr>
<td>hfe(min) @ Ic</td>
<td>20.00</td>
<td>7.00</td>
</tr>
<tr>
<td>Ib = Ic/hfe(min)</td>
<td>4.30</td>
<td>36.75</td>
</tr>
<tr>
<td>Vbe @ Ic</td>
<td>0.84-0.94</td>
<td>1.44-1.48</td>
</tr>
<tr>
<td>Vce(sat) @ Ic</td>
<td>0.20-0.24</td>
<td>1.12</td>
</tr>
</tbody>
</table>

(* Ic of T1) = 4.30 + 36.75

Vce(sat)2(min) = 0.12 + 0.84 = 0.96V

Vce(sat)2(max) = 0.14 + 1.48 = 1.62V
T2 operates in quasi-saturation at all times and is at its minimum only when T1 is fully saturated. T1 is therefore normally over-dimensioned (larger silicon area) to obtain a low value of \( V_{ce(sat)} \) for a given \( I_b \) and \( I_{c1} \).

**Switching Performance of the Power Darlington**

The overall turn off time is given by

\[
T_{off} = T_{s1} + T_{s2} + T_{f2}
\]

During the storage time of T1 (\( T_{s1} \)), \( I_{c2} \) remains constant (Figure 5.6b) as its charge requirements are fulfilled by T1 current flow. T1 eventually turns off and this causes T2 to start consuming its surplus charges at the end of which (\( T_{s2} \)) T2 enters its fall time period and switches off (\( T_{f2} \)). \( T_{s1} \) and \( T_{s2} \) are influenced by:

- the values for \( R_1, R_2 \) which aid charge removal
- the forced gain of T1, T2 which determines the charge storage level in the transistors

Charge removal diodes D1 and D2 conduct only after T1 has turned off and this necessarily means that T2 will turn off in cascade with T1.

**5.2 Transistor Switching Aid Networks**

The use of passive components to protect and reduce electrical stresses in transistors is not a new concept. These networks are required during the switching periods of the cycle when current and voltage transients harmful to the device occur.
Turn-on transients are caused by:

- the use of slow recovery power diodes in the power circuit
- the discharge of stray capacitance and snubber circuits
- stray circuit inductance

Di/dt limiting of transistor current is possible using collector or emitter circuit inductance. This limits the peak transistor current until the circuit attains steady state conditions. It has been shown that the turn on dissipation can be reduced to a third of the unprotected level using di/dt limiting circuitry.

At turn off, voltage transients are produced when interrupting the current in the circuit inductances. Dv/dt limiting circuits (snubbers) are used to divert the load current away from the device, which allows it to switch off under low Vce conditions. Several snubber circuits are shown in Figure 5.9.

In Figure 5.9a, the energy stored in Cs is dissipated in Rs at the next turn on of the transistor. Figure 5.9b,c are non-dissipative snubber circuits that recover the energy stored in Cs. The dissipation in the transistor at turn off is given by (Figure 5.10)

\[ \int_{0}^{T_f} V_{ce} i_c \, dt \] ........(84)

The dissipation in the transistor is reduced by up to 12 times that without the use of a snubber.
Different configurations of the snubber loss reduction network

**FIGURE 5.9a**

- Standard dissipative snubber
- Non-dissipative snubber (requires external components)
- Non-dissipative snubber using passive components only

**FIGURE 5.9c**

Loss recovery network
The device voltage at $t = T_f$ has to be $< V_{ceo}$ giving,

$$Cs > Io.T_f/(2V_{ceo}) \quad \ldots \ldots \ldots (85)$$

In practice, a value of $Vo = 1/2 V_{ceo}$ is recommended to allow for transients due to stray inductance in the snubber circuit. This gives

$$Cs > Io.T_f/V_{ceo} \quad \ldots \ldots \ldots (86)$$

After time $T_f$, $Io$ continues to flow in $Cs$ and the voltage across $Cs$ increases linearly to a peak of $Vo$ where,

$$Vs = 1/Cs \int _t ^{t+T_f} dt + Io.T_f/Cs$$

giving

$$Cs.Vo = Io.T_f/2 + Io. \ldots \ldots \ldots (87)$$

$Vo$ is the maximum voltage across the transistor after it has turned off and needs to be $< V_{ceox}$. The energy stored in $Cs$ is dissipated in $Rs$

$$Ps = 1/2 Cs.Vo .Vo \ldots \ldots \ldots (88)$$

The discharge current at turn on must be limited so that the transistor peak current rating is not exceeded - $Ic(sat) > Vo/Rs + Irm + iL$

where $Irm = Ds$ recovery current

$$iL = \text{transistor current due to the load and flywheel diode}$$

From the data of Figure 4.40 and from equation (86),(87) the transistor $V_{ceo}$ needs to be greater than 200V and $Cs$ greater than 2.57 uF (for $Io = 343A$ $T_f = 1.5 \mu s$)

$Cs$ has also to be of a low dissipation type (e.g. polypropylene dielectric - Figure 5.11)
Transistor waveforms at turn off using a snubber network

FIGURE 5.10

Dissipation curves for snubber capacitors of different dielectric materials

FIGURE 5.11
5.3 Flywheel Diode (Df) Specification

In the chopper configuration, when the transistor is off, Df becomes forward biased and conducts the load current. This only occurs after a delay (< 250 ns) required to establish minority carrier charges in the high resistivity regions of the diode. Once the diode is in conduction, the forward drop is low and dependent on the current through the diode.

When the transistor (T2) is turned on, Df is immediately reverse biased and its current commutates to T2. The rate of current transfer is limited by d(IT)/dt.

At the end of forward conduction a reverse current flows in the diode, corresponding to a removal of the minority carrier charges stored in the diode. Some of the charges are removed by recombination and the rest by reverse current flow in the diode - Figure 5.12a.

During the first part of the recovery, the circuit imposes the d(IF)/dt. The peak reverse current (Irm) flows through T2. The recovered charge in this period is reduced with decreasing d(IF)/dt (Figure 5.12b).

The forward recovery current and time are given by:

\[ t_{rr} \approx \sqrt{3.\frac{Q_{rr}}{d(\text{IF})/dt}} \]  \hspace{1cm} \text{(91)}

\[ I_{rm} \approx \sqrt{\frac{1}{4.3.\frac{Q_{rr}}{d(\text{IF})/dt}}} \]  \hspace{1cm} \text{(92)}

During the forward recovery period, the transistor supports the full supply voltage (\(V_1 - V_f\)) and is hence operating in the linear mode. The high dissipation in the transistor during this period cannot be neglected, especially for high frequency (15kHz) operation.
Flywheel diode (Df) waveforms during its recovery period

FIGURE 5.12a

Relationship between $Q_{rr}$ and $\frac{d(iF)}{dt}$

FIGURE 5.12b
The second part of the recovery reduces the reverse current in Df to zero. Diodes with soft recovery profiles are preferred as the resulting di/dt is device dependent and if too high cause high reverse voltages across the diode.

40

Power Loss:

Forward conduction loss  = Vf.iF.Toff.Fo  ...(93)

Reverse recovery loss  = Qrr.Vi x Fo  ...(94)

Voltage surges across Df:

The reverse recovery d(Irr)/dt produces a transient voltage (Lstray.d(Irr)/dt) across the diode at the end of the reverse recovery period.

The voltage across Df = Vi + Lstray.d(Irr)/dt ....(95)

An R-C network of 0.1 uf/1.0JΩ is fitted across Df to damp out the transients.

5.4 Transistor Base Drive Requirements

The base drive requirements for the transistor are:

a) Forward bias mode:
   - base current (Ib) overshoot at turn on in order to rapidly saturate the transistor and maintain its saturation during the turn on transient phase
   - a fast rise in Ib ( < 250 nS to its peak value)
   - sufficient base current to maintain the device in saturation under worst case load conditions
b) Reverse bias mode:
   - apply a negative bias to the base-emitter
     junction for charge removal from the device
     during the storage and fall time periods
   - maintain the base-emitter in the cut-off state
     after the turn-off period

c) provide galvanic isolation between the control and
   power stages

d) have a facility for adaptive de-saturation of the
   device during the turn-off phase

e) incorporate device overcurrent protection

When a voltage source is used to forward bias the
transistor, the base current cannot increase to its
full value during the base resistance modulation stage.
The device will therefore experience high losses as it
cannot be fully saturated rapidly. Current sourced
forward bias circuits impose a base current on the
base-emitter junction and are preferred to voltage
sourced base drives.

Storage time reduction is possible by maintaining the
transistor in quasi-saturation using an anti-
saturation diode (Figure 5.13a). The disadvantage of
this method is that the saturation losses in the device
are increased which can be significant for high current
operation. An alternative approach is to allow the
device to fully saturate and then force it to de-saturate
prior to applying reverse bias to its base-emitter
junction (Figure 5.13b). When operating in the Darlington
Da — Vce (min) = 0.7v

Vce clamping using an anti-saturation diode

**FIGURE 5.13a**

Transistor actively desaturated prior to applying Vbe reverse bias

**FIGURE 5.13b**
mode, the output device is always in quasi-saturation but still requires controlled charge removal techniques in order to optimise transistor turn off times.
At least -2.5V of reverse bias is required across the base-emitter junction of a Darlington transistor to ensure that the device is fully cut-off.

5.4.1 Base Drive Circuit Design

Circuit Description

With reference to Figure 5.14, the circuit operates from a ±7V supply generated by a dc-dc converter. The converter is supplied from the main capacitor bank used to supply the power transistors (60V d.c.). This provides additional protection to the transistors during power failure as the base drive circuit will continue to operate until the main capacitor bank discharges. A simple flyback type of converter consisting of IC1, TX1 and TR5 produces ±10V d.c. which is then regulated by REG1 and REG2. The converter runs at 33kHz and with a 50% duty cycle. D4 resets TX1 when the converter is lightly loaded. The pulsewidth modulated signals are fed to the pulse steering circuit formed by IC4. A high level at PL1/10 enables the constant current source (TR1). A high level at PL1/9 turns TR1 off and TR2 on. The latter reverse biases the driver stage of the Darlington switch. When the Darlington comes out of saturation, Vce detect comparator (IC2) switches TR3 ON to provide the Darlington output device (T2) with
Base drive circuit

**FIGURE 5.14**
reverse bias. Waveforms for the base drive outputs
B1, B2 are shown in Figure 5.15. The initial overshoot
of current is produced by C30. The circuit provides
±1A at B1 and up to -25A at B2.

Summary of Base Drive Circuit Design
- a current sourced 1 Ampere forward bias is used to
turn the Darlington on
- a 5us overshoot in Ib achieves fast saturation of
the Darlington
- the driver and output stages of the Darlington are
reverse biased separately
- a de-saturation detect circuit is used to obtain
optimised turn-off times

5.5 Results of experiments carried out on the Power Modules

The experimental Power Modules (PM) were built using
the following components:

- Output Transistor (T2) 3 off ESM3001 [Thomson CSF]
- Driver Transistor (T1) TC40U [Marconi MEDL]
- Flywheel Diode (Df) R6221230PS [Westinghouse]
- Snubber Diode (Ds) BYW78/200
- Collector Diode (Dc) BYX65/300
- Snubber Capacitor (Cs) RIFA PHU483V725/ and
  ICW 4.0u/120V
- Heatsinks (for T2) EDN250 [MEDL]
- Heatsink (for Df) EDN150 [MEDL]
- Snubber Resistance (Rs) 2x0R3/90Watts (2.2uHx0R3)
- Collector Resistance(Rc) 1x0R3/90Watts (2.2uHx0R3)
- Collector Inductance(Lc) 0.5uH/200A
Transistor base-emitter waveforms at turn-on

Configuration: Darlington

FIGURE 5.15
Snubber Inductance (Ls)  2.2uH/75A
Output Inductance (Lf)  60uH/250A
R-C Diode suppression  1R0/2W metal oxide,
                   0.1uF/1000V polyprop

5.5.1 Power Module Construction

Several attempts were made at achieving a component layout which met the following requirement:

i) minimal cable/interconnecting inductance

ii) unrestricted air flow across all the power components

iii) access for the insertion of current probes

for the measurement of currents iT,IF,ic,iS,iz

iv) access to all devices for temperature measurement using contacting thermocouple probes

The final layout is shown in Figure 5.16. The power transistors are directly coupled by an aluminium busbar which extends to the cathode terminal of Df. This ensures a low emitter stray inductance connection. Collector inductor Lc is connected directly to the filter capacitor bank and to T2 collector. The air flow across the power module varies from 5.0 - 7.5 metres/s.

Test Rig Description

The power module test rig (Figure 5.17) consisted of a 65V d.c. supply with 120,000 uF capacitor filtering. The supply regulation was 1.5V/100A up to 500A. The output of the PM was loaded using a variable resistance (0.060 - 6.0 ohms) load bank.
FIGURE 5.16

Layout of the 250A power module components

Dz and Rz mounting plate
({ devices underneath})

connections to base drive circuit

3 x T2

Lc

Rc

mounting plate

Rs

Lf

Df heatsink

C3

Ds
Schematic of power module test rig

FIGURE 5.17
Test Equipment:
Current Probe type Tektronix AM503/P6303/P6302/CT5
Oscilloscope type Philips PM3715, 60MHz, Dual timebase
Oscilloscope camera Shackman type B20
U.V. recorder type Medelec "M" Scope 4 Channel Fibre optic strip chart recorder

5.5.2 General Power Circuit Waveforms - Figure 5.18

Current and voltage waveforms at different parts of the circuit are shown in P1. The transfer of current from Df to T2 at the start of a new cycle occurs in approximately 2 μs. At this stage Cs discharges through T2, Ls and Rs. The peak discharge current (iS) occurs 4.6 μs after transistor turn on. Cs commences a resonant charging cycle through the load (constant current) after 8.4 μs and this causes a reciprocal change in T2 current (load current is constant). The peak transistor current occurs in the first 3 μs of the cycle.
P2 shows the snubber current, charging Cs prior to turn on, transferring into T2 at turn on. P3 is taken at a different pulse width where the snubber was discharging Cs resonantly prior to T2 turning on. The peak discharge current is higher in P2 (70A) than in P3 (64A) and varies with the pulsewidth.

Turn off waveforms are shown in Figure 5.19. In P4, the current in T2 transfers to Cs during the fall time period. Df does not conduct any current until iS starts to decrease (P6). The energy stored in Lc and circuit emitter and collector stray inductance is transferred.
General circuit waveforms at turn on

FIGURE 5.18
General circuit waveforms at transistor turn off

FIGURE 5.19

- P4:
  - $i_T = 160\text{A/div}$
  - $i_C = 160\text{A/div}$
  - $i_S = 80\text{A/div}$
  - $i_F = 160\text{A/div}$
  - T.B. 10us/div

- P5:
  - Vce 50v/div
  - $i_C = 80\text{A/div}$
  - T.B. 2us/div
  - $i_T = 80\text{A/div}$

- P6:
  - $i_T = 160\text{A/div}$
  - $i_C = 160\text{A/div}$
  - $i_S = 80\text{A/div}$
  - $i_F = 160\text{A/div}$
  - T.B. 2us/div
to Cs, with a corresponding increase in $V_{ce}$ (P5). When $V_{ce}$ exceeds $V_z$, $D_z$ conducts. $i_z$ peaks at 50A and then reduces as $V_{ce}$ starts to decrease.

5.5.3 Transistor Switching Waveforms

One cycle (at 15kHz) of T2 current and voltage waveforms are shown in Figures 5.20, 5.21, 5.22. The main features of the waveforms are:

- P7; T2 peak current occurs during the recovery of Df
- P8, P9; T2 stays out of saturation until Df has recovered to its blocking state
- P10, Vce of T2 increases during the fall time period (Tf) due to stray inductance effects
- a 5MHz oscillation is observed on the Vce trace; this occurs immediately after T2 current is zero; the onset of this oscillation marks the end of T2 conduction; this abrupt interruption of current in the emitter and collector circuit is the cause of the oscillation and is due to a resonance between the circuit stray capacitances and inductances.
- P11, P12; Vce increases to 115V as Lc discharges into Cs. $D_z$ conducts and limits Vce to 135V. $i_z$ and iT are measured at the same junction and hence appear on the same trace
- P12; the three devices in parallel have a total $T_f = 0.8 \mu s @ 160A \ (d(iT)/dt = 200A/\mu s)$
- P13a,b; the Vce x iT trace shows the devices operating within the SOAR boundaries specified by the manufacturers
Transistor turn on waveforms

**FIGURE 5.20**

- **P7**
  - iF = 40A/div
  - T.B. 5us/div
  - iT = 40A/div

- **P8**
  - Vce = 20v/div

- **P9**
  - Vce = 50v/div
  - iT = 80A/div
  - T.B. 2us/div
Transistor turn-off waveforms

Vce 50v/div
iT 80A/div
T.B. 1us/div

Dz limits Vce
Vce 50v/Div
T.B. 1us/div

iT 40A/div
T.B. 1us/div
iz shown on iT trace ( x )

FIGURE 5.21
Safe Operating Area for the ESM3001 Transistor

*SOAR limits for the ESM3001

FIGURE 5.22
5.5.4 Optimisation of Transistor Turn-Off

The minority carrier charge stored in the transistors will vary from device to device due to the spread in resistivity of the semiconductor materials and diffusion characteristics. \( T_f \) can be optimised by applying a reverse bias to \( T_2 \) only after it is in quasi-saturation. Some experimentation was carried out to determine the most suitable form of reverse bias circuit for the ESM3001 transistor.

Optimisation of de-saturation turn-off method (Figure 5.23, 5.24)

On receiving the turn off signal, the base-emitter of driver transistor, \( T_1 \), is reversed biased immediately. \( T_2 \), however, is allowed to de-saturate before being reverse biased. Direct application of reverse bias to \( T_2 \) is delayed by \( R_{29}, C_{26} \) (Figure 5.14), the delay time needs to be longer than the storage time of \( T_2 \).

P14, P15, P16 show the effect of varying the delay from 0.5 to 12 \( \mu \)S. The total turn off time (measured from the time \( T_1 \) is reversed biased to the time \( T_2 \) current is zero) is extended by 1.6\( \mu \)S using the de-saturation method (Figure 5.23a). However, the charge recovered from \( T_2 \) is reduced from 14\( \mu \)C to 6\( \mu \)C. The 8\( \mu \)C reduction in the extracted charge has been used up by \( T_2 \) in conducting its load current during the enforced storage time. Fall times are improved from 2.2\( \mu \)S to 1.4 \( \mu \)S. Note that increasing the delay beyond 4\( \mu \)S does not improve the switching performance as the \( V_{ce} \) detect circuit is already in control of \( T_2 \) turn off (P15, P16.)
Also note that the Vbe of T2 is held at a positive level whilst T1 is still conducting. Base-emitter diodes D1, D2, D3, are not reversed biased until T1 turns off. These diodes then conduct T2 reverse bias currents. The reverse bias diodes can be connected either to the base of T1 or returned directly to a separate negative supply as shown in Figures 5.23b, c. These configurations are referred to as the series and parallel reverse bias systems.

**Parallel Reverse Bias of T1, T2 (Figure 5.23b)**

In the parallel reverse bias system, Ib1 removes stored charges from T1 only. Ib2 diverts current from T1 emitter away from the base of T2 and also removes stored charges from T2. Ib1, Ib2 are allowed to flow simultaneously producing the waveforms of Figure 5.24. The disadvantage of this turn off method is that T1 can be forward biased if the reverse bias applied to T2 base is more negative than that applied to T1 base.

**Series Reverse Bias of T1 and T2 (Figure 5.25)**

By connecting D1, D2, D3 to the base of T1 (Figure 5.23c) T2 is forced to turn off after T1. The reverse base current (P17) shows two stages of charge removal corresponding to T1 and T2 turning off sequentially. In the series method, charge removal from T2 takes place initially at terminal B1 (P18) and after desaturation at B2. In the parallel method no charge removal from T2 takes place until T2 desaturates (P19).
Transistor turn off time optimisation using active desaturation technique

FIGURE 5.23a

Parallel Reverse Bias Circuit
Figure 5.23b

Vbe = Vbe1 + Vbe2

Series Reverse Bias Circuit
Figure 5.23c
Optimisation of transistor current fall time
( using parallel reverse bias method )

**FIGURE 5.24**

- **P14**
  - $i_b = 2 \text{A/div}$
  - $i_T = 280 \text{A/div}$
  - T.B. $1 \text{us/div}$
  - $V_{be} = 5 \text{v/div}$
  - $Q_c = 14 \mu \text{C}; T_{dr} = 0.5 \mu \text{s}$

- **P15**
  - $i_b = 2 \text{A/div}$
  - $i_T = 280 \text{A/div}$
  - T.B. $1 \text{us/div}$
  - $V_{be} = 5 \text{v/div}$
  - $Q_c = 6 \mu \text{C}; T_{dr} = 4 \mu \text{s}$

- **P16**
  - $i_b = 2 \text{A/div}$
  - $i_T = 280 \text{A/div}$
  - T.B. $1 \text{us/div}$
  - $V_{be} = 5 \text{v/div}$
  - $Q_c = 6 \mu \text{C}; T_{dr} = 12 \mu \text{s}$
  - $T_{dr} = \text{desaturation delay}$
Series reverse bias method waveforms

FIGURE 5.25
Comparison between driver and output transistor collector currents

FIGURE 5.26
When T2 de-saturates, the remaining charges are removed at terminal B2.

In the parallel method, no charge extraction of T2 takes place until Ib2 flow is enabled by the Vce detect circuit. In both cases, the collector current fall time of T2 is about 1.4μS. With the series method, the base-emitter voltages of T1 and T2 during reverse bias are such that T2 cannot be transiently forward biased as in the parallel method. The series method was therefore preferred. P20 to P22 of Figure 5.26 show the relationship between the currents in T1 and T2 of the Darlington configuration.

5.5.5 Optimisation of Snubber Component Values

The snubber circuit is required to limit the dv/dt at turn off to less than 50V/μS. It has been shown (Figure 4.21) that the rapid fall of transistor current \[ \frac{d(i_T)}{dt} > 150A/\mu S \] causes an uncontrolled increase in Vce during the fall time period, due to the effects of circuit and component stray inductances. The self-inductance of Cs and the interconnecting lead inductances need to be minimised. Cs was changed to the ICW/4uF type and was mounted directly (Figure 5.16) onto the emitter busbar of T2. This reduced Lxs to 0.3uH. For the circuit of Figure 5.27, the peak snubber discharge current at turn on is given by (assuming Rs is negligible)

\[
i_S = \frac{V_i}{\sqrt{\frac{C_s}{L_s + L_{xs}}}} \quad \text{...(96)}
\]
where \( L_{xs} \) = stray inductance of the snubber circuit.

The time taken to fully discharge \( C_s \) (first resonant discharge) is

\[
T_{ds} = \frac{2.11}{\sqrt{C_s(L_s + L_{xs})}} \quad \ldots (97)
\]

\( L_{xs} \) was measured (0.8uH) in circuit using an inductance bridge.

\( i_s \) was measured (@ \( i_L = 50A \)) and compared against values obtained from (96) above.

For \( C_s = 3.0\mu F, V_c = 88V \),

<table>
<thead>
<tr>
<th>( L_s ) (( \mu H ))</th>
<th>( L_{xs} ) (( \mu H ))</th>
<th>( T_{ds} ) (( \mu s ))</th>
<th>( i_s ) (A)</th>
<th>( T_{ds} ) (( \mu s ))</th>
<th>( i_s ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.7 )</td>
<td>( 0.8 )</td>
<td>( 3.3 )</td>
<td>( 124 )</td>
<td>( 4.8 )</td>
<td>( 116 )</td>
</tr>
<tr>
<td>( 1.1 )</td>
<td>( 0.8 )</td>
<td>( 3.8 )</td>
<td>( 110 )</td>
<td>( 5.2 )</td>
<td>( 100 )</td>
</tr>
<tr>
<td>( 1.9 )</td>
<td>( 0.8 )</td>
<td>( 4.5 )</td>
<td>( 93 )</td>
<td>( 6.5 )</td>
<td>( 84 )</td>
</tr>
</tbody>
</table>

The discrepancy between the measured and calculated values of \( T_{ds} \) are probably due to the assumptions made in neglecting the effects of \( R_s \). A compromise between \( i_s \) and \( T_{ds} \) is required to ensure that \( C_s \) is fully discharged within the minimum pulsewidth (5\( \mu s \)). The self-inductance of \( R_s \) needs to be considered as these vary with the type of resistor chosen e.g.

- **wirewound type** 0.5 ohm (10.0\( \mu H \))
- **metalclad type** 0.5 ohm (2.0\( \mu H \))
- **tapewound type** 0.5 ohm (2.2\( \mu H \))

Tape wound resistors were preferred as they can operate at higher temperatures without any heatsinking.
Snubber circuit current and voltage waveforms

snubber diode voltage
50v/div

snubber diode current
40A/div
T.B. 10μs/div

Snubber capacitor current
40A/div
T.B. 10μs/div

Snubber discharge path in circuit

FIGURE 5.27
The performance of the snubber circuit for \( I_{ref} = 200A \) is shown in P25, P26 (Figure 5.27).

5.5.6 Flywheel Diode (Df) Test Results

The relationship between \( i_T, i_S \) and \( i_F \) was shown in P1. At the commencement of the cycle, \( i_F \) commutates to \( T_2 \) and a reverse recovery current flows in \( D_f \) and \( T_2 \). Tests were performed on three diodes from different manufacturers and the results are summarised in Figure 5.28a, b. In all cases, the circuit and load conditions were the same \([d(i_F)/dt,i_F]\). The peak recovery current (\( I_{rm} \)) and recovered charge (\( Q_{rr} \)) showed a spread of 44-60A and 21-70uC respectively, between the best and worst of the devices. The WE62212030 also exhibits a soft recovery characteristic, (Figure 5.29, P27), which is preferable. P28 shows the voltage across \( D_f \) during the commutation period. During the forward recovery phase, \( V_f \) is negative but swings rapidly to 90V during the reverse recovery period. The transient voltage is the product of stray circuit inductance and the high \( d(I_{rr})/dt \). The \( d(V_f)/dt \) is about 900V/\( \mu \)S.

5.6 Results of Power Module Tests up to 250A Output

Five Power Modules were built and tested as part of the development programme, using ESM1000, ESM3001 and DT63 Transistors (Appendix B). With reference to Figure 5.30, as \( I_{ref} \) is varied from between 75 to 250A,
$I_{ref} = 200A$

<table>
<thead>
<tr>
<th>Device Type</th>
<th>R603 122HS</th>
<th>SM02 PHR170</th>
<th>251 UL0515</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>(WE)</td>
<td>Westcode</td>
<td>I.R.</td>
</tr>
<tr>
<td>$d(iF)/dt$ A/us</td>
<td>68.00</td>
<td>57.0</td>
<td>65.0</td>
</tr>
<tr>
<td>$iF$</td>
<td>160.00</td>
<td>160.0</td>
<td>160.0</td>
</tr>
<tr>
<td>$Toff$ (us)</td>
<td>20.00</td>
<td>20.0</td>
<td>20.0</td>
</tr>
<tr>
<td>$I_{rm}$</td>
<td>44.00</td>
<td>48.0</td>
<td>60.0</td>
</tr>
<tr>
<td>$t_{fr}$ (us)</td>
<td>0.75</td>
<td>0.8</td>
<td>1.2</td>
</tr>
<tr>
<td>$t_{rr}$ (us)</td>
<td>0.20</td>
<td>5.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$V_F$</td>
<td>2.40</td>
<td>3.0</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_R$</td>
<td>120.00</td>
<td>80.0</td>
<td>110.0</td>
</tr>
<tr>
<td>$\theta_d$ C</td>
<td>37.00</td>
<td>48.0</td>
<td>39.0</td>
</tr>
<tr>
<td>$V_1$</td>
<td>6.00</td>
<td>7.5</td>
<td>9.0</td>
</tr>
<tr>
<td>$V_2$</td>
<td>8.00</td>
<td>20.0</td>
<td>10.0</td>
</tr>
<tr>
<td>$Q_{rr}$ (uC)</td>
<td>20.90</td>
<td>40.0</td>
<td>70.0</td>
</tr>
<tr>
<td>$P_d$</td>
<td>170.00</td>
<td>225.0</td>
<td>189.0</td>
</tr>
</tbody>
</table>

$Toff = D_f \text{ conduction time}$

$\theta_d = D_f \text{ case temperature}$

Comparison between 3 Fast Recovery Diodes

**FIGURE 5.28a**
<table>
<thead>
<tr>
<th>Parameter</th>
<th>50</th>
<th>100</th>
<th>150</th>
<th>175</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iref</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>d(IF)/dt (A/us)</td>
<td>80.0</td>
<td>75.0</td>
<td>64.0</td>
<td>57.50</td>
<td>62.00</td>
</tr>
<tr>
<td>IF</td>
<td>48.0</td>
<td>100.0</td>
<td>136.0</td>
<td>136.00</td>
<td>160.00</td>
</tr>
<tr>
<td>Toff (us)</td>
<td>52.0</td>
<td>44.0</td>
<td>36.0</td>
<td>28.00</td>
<td>24.00</td>
</tr>
<tr>
<td>Irm</td>
<td>40.0</td>
<td>40.0</td>
<td>40.0</td>
<td>44.00</td>
<td>44.00</td>
</tr>
<tr>
<td>tfr (us)</td>
<td>0.6</td>
<td>0.6</td>
<td>0.60</td>
<td>0.60</td>
<td>0.70</td>
</tr>
<tr>
<td>trr (us)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.15</td>
<td>0.15</td>
<td>0.25</td>
</tr>
<tr>
<td>Vf</td>
<td>2.4</td>
<td>2.4</td>
<td>2.40</td>
<td>2.40</td>
<td>2.40</td>
</tr>
<tr>
<td>Vr</td>
<td>100.0</td>
<td>100.0</td>
<td>100.0</td>
<td>100.00</td>
<td>100.00</td>
</tr>
<tr>
<td>Od C</td>
<td>25.6</td>
<td>32.0</td>
<td>35.50</td>
<td>36.00</td>
<td>38.00</td>
</tr>
<tr>
<td>V1</td>
<td>4.0</td>
<td>4.4</td>
<td>4.00</td>
<td>6.00</td>
<td>3.00</td>
</tr>
<tr>
<td>V2</td>
<td>5.0</td>
<td>6.0</td>
<td>5.00</td>
<td>8.00</td>
<td>7.50</td>
</tr>
<tr>
<td>Qrr (uC)</td>
<td>14.0</td>
<td>14.0</td>
<td>15.00</td>
<td>16.50</td>
<td>20.90</td>
</tr>
</tbody>
</table>

Od = Df case temperature

Toff = Df conduction time

Tests on Westinghouse R622 Fast Recovery Diode

FIGURE 5.28b
Theoretical waveforms for Df operation

FIGURE 5.29a

Flywheel diode (Df) waveforms

FIGURE 5.29b
- the current fall time of T2 varies from 0.4 to 1.5μS. Between 200A and 250A, Tf shows a large increase which corresponds to a similar increase in the device case temperature.
- Vce(pk) increases to between 85 and 148V (Vi = 60V)

The above results were for load currents up to 200A continuous and at a 50% duty cycle (250A @ 15 secs, 100A @ 15 secs) for 250A operation.

The data for the 5 modules for Iref values of 200A and 250A are summarised in Figures 5.31, 5.32, respectively. The saturation voltages are significantly different between the ESM1000, the ESM3001 and DT63 transistors. This is because the ESM1000 has a smaller chip area (Ic(sat) = 100A) and hence a higher Vce(sat) for a given current. The ESM3001 is a manufacturer's replacement device for the ESM1000 whilst the DT63 is a higher current device than the ESM3001, with a larger silicon area and lower Vce(sat).

A wide variation in peak transistor currents are observed. This could occur for a number of reasons:
- the flywheel diode recovery characteristics are necessarily different between the modules yielding different values of Irm
- the contribution of snubber discharge current at turn on will vary with stray inductance, pulsewidth (P2, P3 Figure 5.18) and the tolerance of the inductance Lc
In Figure 5.32, the longer fall time of the DT63 devices has the effect of increasing \( V_{ce(pk)} \) (at turn off) and \( i_T \) (at turn on) compared to the modules using ESM devices. Being a higher voltage device, the stored charge level in the DT63 is higher with a corresponding increase in current fall times. In the 200A and 250A tests, the model data is pessimistic compared to actual measurements.

5.6.1 Load Current Waveforms:

The load current waveforms into a resistive load are shown in Figure 5.33 (P29 to P33). The current ripple is 17A p/p @ 15kHz. Pulse rise and fall times are 0.5 ms. The effect on the output current of varying \( L_f \) are summarised in Figure 5.34.

5.6.2 Short Circuit Load Tests:

The current control system has been designed to maintain regulation into a short circuit (\( RL \to 0 \)). The pulsewidth reduces (@ 15kHz) to maintain regulation until it reaches 5us (minimum on time). If lower pulsewidths are demanded by the current loop, the frequency is reduced (@ 5us pulsewidth)

Figure 5.23. Current regulation curves are shown in Figure 5.35. Short circuit voltages of 0.2V (50A) and 0.7V (200A) were the minimum achievable with one 2 metre of 50mm copper cable as the load.
<table>
<thead>
<tr>
<th></th>
<th>75</th>
<th>100</th>
<th>150</th>
<th>200</th>
<th>250</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iref (A)</td>
<td>75.00</td>
<td>100.00</td>
<td>150.00</td>
<td>200.00</td>
<td>250.00</td>
</tr>
<tr>
<td>Tr (us)</td>
<td>3.00</td>
<td>3.50</td>
<td>4.00</td>
<td>5.00</td>
<td>6.00</td>
</tr>
<tr>
<td>iT(pk) (A)</td>
<td>160.00</td>
<td>172.00</td>
<td>232.00</td>
<td>250.00</td>
<td>280.00</td>
</tr>
<tr>
<td>iT(Tf) (A)</td>
<td>80.00</td>
<td>96.00</td>
<td>140.00</td>
<td>184.00</td>
<td>180.00</td>
</tr>
<tr>
<td>Vce(Tr) (V)</td>
<td>5.00</td>
<td>4.00</td>
<td>3.50</td>
<td>3.80</td>
<td>6.50</td>
</tr>
<tr>
<td>Vce(sat) (V)</td>
<td>2.00</td>
<td>3.50</td>
<td>3.00</td>
<td>3.00</td>
<td>2.50</td>
</tr>
<tr>
<td>Tf (us)</td>
<td>0.40</td>
<td>0.50</td>
<td>0.50</td>
<td>1.10</td>
<td>1.50</td>
</tr>
<tr>
<td>Vce(Tf)</td>
<td>60.00</td>
<td>64.00</td>
<td>68.00</td>
<td>60.00</td>
<td>70.00</td>
</tr>
<tr>
<td>Vce(pk)</td>
<td>85.00</td>
<td>92.00</td>
<td>120.00</td>
<td>148.00</td>
<td>140.00</td>
</tr>
<tr>
<td>TC1</td>
<td>30.00</td>
<td>33.00</td>
<td>39.00</td>
<td>50.00</td>
<td>72.00</td>
</tr>
<tr>
<td>TC2</td>
<td>29.60</td>
<td>33.50</td>
<td>42.00</td>
<td>46.00</td>
<td>71.00</td>
</tr>
<tr>
<td>TC3</td>
<td>30.00</td>
<td>35.50</td>
<td>42.50</td>
<td>49.00</td>
<td>76.00</td>
</tr>
<tr>
<td>ød C</td>
<td>29.30</td>
<td>30.70</td>
<td>36.00</td>
<td>45.00</td>
<td>38.00</td>
</tr>
<tr>
<td>Tamb C</td>
<td>26.80</td>
<td>27.50</td>
<td>26.50</td>
<td>31.00</td>
<td>32.00</td>
</tr>
<tr>
<td>Pulsewidth (us)</td>
<td>18.75</td>
<td>25.00</td>
<td>37.50</td>
<td>50.00</td>
<td>62.50</td>
</tr>
</tbody>
</table>

Device: ESM1000 (3 off)

Frequency: 15kHz

TC1, TC2, TC3 = transistor case temperatures (°C)

ød = Df case temperature

Power Module 1 Results for Iref = 50 to 250A

FIGURE 5.30
<table>
<thead>
<tr>
<th>Power Module No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width (us)</td>
<td>48.0</td>
<td>48.0</td>
<td>48.0</td>
<td>48.0</td>
<td>48.0</td>
</tr>
<tr>
<td>Tr (us)</td>
<td>5.0</td>
<td>5.0</td>
<td>6.0</td>
<td>6.0</td>
<td>4.5</td>
</tr>
<tr>
<td>iT(pk) (A)</td>
<td>250.0</td>
<td>200.0</td>
<td>200.0</td>
<td>176.0</td>
<td>192.0</td>
</tr>
<tr>
<td>Vce(Tr) (V)</td>
<td>6.0</td>
<td>5.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vce(sat) (V)</td>
<td>3.0</td>
<td>2.8</td>
<td>1.0</td>
<td>1.0</td>
<td>0.8</td>
</tr>
<tr>
<td>iT(Tf) (A)</td>
<td>184.0</td>
<td>170.0</td>
<td>176.0</td>
<td>168.0</td>
<td>144.0</td>
</tr>
<tr>
<td>Vce(Tf) (V)</td>
<td>60.0</td>
<td>84.0</td>
<td>60.0</td>
<td>170.0</td>
<td>70.0</td>
</tr>
<tr>
<td>Vce(pk) (V)</td>
<td>148.0</td>
<td>136.0</td>
<td>150.0</td>
<td>135.0</td>
<td>155.0</td>
</tr>
<tr>
<td>TC1</td>
<td>50.0</td>
<td>49.0</td>
<td>44.0</td>
<td>43.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TC2</td>
<td>46.0</td>
<td>49.0</td>
<td>54.0</td>
<td>39.0</td>
<td>60.0</td>
</tr>
<tr>
<td>TC3</td>
<td>49.0</td>
<td>53.0</td>
<td>50.0</td>
<td>47.0</td>
<td>-</td>
</tr>
<tr>
<td>Tf (us)</td>
<td>1.1</td>
<td>1.0</td>
<td>1.4</td>
<td>0.8</td>
<td>2.0</td>
</tr>
<tr>
<td>θd C</td>
<td>45.0</td>
<td>45.0</td>
<td>50.0</td>
<td>43.5</td>
<td>57.0</td>
</tr>
<tr>
<td>Tamb C</td>
<td>28.0</td>
<td>20.5</td>
<td>22.5</td>
<td>22.5</td>
<td>21.3</td>
</tr>
<tr>
<td>Transistor type:</td>
<td>ESM1000</td>
<td>ESM3001</td>
<td>DT63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. off</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TC1, TC2, TC3 = Transistor case temperatures (°C)

θd = Df case temperature

Fo = 15kHz

Results for Power Modules No. 1-5 @ Iref = 200A

FIGURE 5.31
<table>
<thead>
<tr>
<th>Power Module No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>Model Prediction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Width-μs</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td></td>
</tr>
<tr>
<td>Tr (μs)</td>
<td>6.0</td>
<td>55</td>
<td>8.0</td>
<td>8.00</td>
<td>6.0</td>
<td>3.2</td>
</tr>
<tr>
<td>iT(Tr) (A)</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>298</td>
<td>343</td>
</tr>
<tr>
<td>Vce(sat) (V)</td>
<td>2.5</td>
<td>3</td>
<td>1.3</td>
<td>1.25</td>
<td>0.9</td>
<td>3.0</td>
</tr>
<tr>
<td>iT(Tf) (A)</td>
<td>180.0</td>
<td>200</td>
<td>200.0</td>
<td>184.00</td>
<td>176.0</td>
<td>256</td>
</tr>
<tr>
<td>Vce(Tf) (V)</td>
<td>70.0</td>
<td>60</td>
<td>60.0</td>
<td>130.00</td>
<td>60.0</td>
<td>130</td>
</tr>
<tr>
<td>Vce(pk) (V)</td>
<td>140.0</td>
<td>140</td>
<td>165.0</td>
<td>145.00</td>
<td>165.0</td>
<td>187</td>
</tr>
<tr>
<td>TC1</td>
<td>72.0</td>
<td>67</td>
<td>48.0</td>
<td>51.00</td>
<td>73.0</td>
<td>&lt;-----</td>
</tr>
<tr>
<td>TC2</td>
<td>71.0</td>
<td>60</td>
<td>82.0</td>
<td>51.00</td>
<td>71.0</td>
<td>51.3</td>
</tr>
<tr>
<td>TC3</td>
<td>76.0</td>
<td>67</td>
<td>54.0</td>
<td>63.00</td>
<td>&lt;-----</td>
<td></td>
</tr>
<tr>
<td>Tf (μs)</td>
<td>1.5</td>
<td>1</td>
<td>2.0</td>
<td>1.00</td>
<td>2.8</td>
<td>&lt;-----</td>
</tr>
<tr>
<td>θd (°C)</td>
<td>62.0</td>
<td>41</td>
<td>46.0</td>
<td>54.00</td>
<td>72.0</td>
<td>146</td>
</tr>
<tr>
<td>Tamb (°C)</td>
<td>22.5</td>
<td>23</td>
<td>21.0</td>
<td>20.00</td>
<td>23.5</td>
<td>33</td>
</tr>
</tbody>
</table>

Transistor type: <-ESM1000-> <-ESM3001-> DT63

No. off: 3 3

TC1, TC2, TC3 = transistor case temperature (°C)

θd = Df case temperature

Fo = 15kHz

Results for Power Modules No. 1-5 @ Iref = 250A

FIGURE 5.32
Load current waveforms for the 250A power module (resistive load)

200A
iL 32A/div
100A
ripple = 17A
F = 50Hz

200A
Pulse rise period
100A
T.B. 0.5ms/div

200A
Pulse decay period
100A
T.B. 0.5ms/div

FIGURE 5.33
<table>
<thead>
<tr>
<th>Inductance (µH)</th>
<th>50</th>
<th>60</th>
<th>75</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple p/p (A)</td>
<td>22.00</td>
<td>16.0</td>
<td>12.8</td>
<td>9.6</td>
</tr>
<tr>
<td>tR (ms)</td>
<td>0.75</td>
<td>0.8</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>tF (ms)</td>
<td>0.50</td>
<td>1.0</td>
<td>1.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

**Actual Measurements**

| Ripple p/p (A)  | 12.1 | 10.1 | 8.1 | 6.1 |
| tR (ms)         | 0.4 | 0.47 | 0.6 | 0.8 |
| tF (ms)         | -   | -   | -   | -   |

**Model predictions (data from Appendix A)**

- tr = current rise time in pulsed operation
- tF = current fall time in pulsed operation

Pulsed operation: Ip = 250; Ib = 50A; parameters frequency = 200Hz @ 50% duty cycle

**Effect of Varying Lf**

FIGURE 5.34
Output current regulation curves for the 250A power module

RL varied from 1 ohm to 0.01 ohms

FIGURE 5.35
5.7 Parallel, Bi-phase Operation of two Power Modules

To obtain the 500A output required for the power source, two 250A power modules were connected in parallel. The ripple content of the output can be reduced by operating the power modules carrier frequencies (Fo) 180 degrees out of phase. The ripple amplitude varies with the pulsewidth, minimum ripple occurring when the pulsewidth is 50% (Figure 5.36). The ripple frequency is 30kHz (2 x Fo).

Load current measurements for the modules are summarised in Figure 5.37. Individual modules show ripple amplitudes of up to 20A p/p compared to a maximum of 3A p/p for the modules in parallel.

5.7.1 Current sharing between Power Modules

Figure 5.37 showed an imbalance of current between the two modules operating in parallel (\(\nabla i\)). Further investigation revealed that the load current contribution from each module was influenced by:

- device Vce(sat) where a difference of 0.25V in the Vce(sat) values will produce a mismatch of 5A and 50A into a load of 0.05 and 0.005 ohm respectively (corresponding to a normal arc and short circuit arc load)

- the snubber current amplitude which is a function of Ls, Cs, Rs; a variation in the values of these between the modules will contribute to the current imbalance

- the flywheel diode conduction voltage drop (Vf) and filter inductance (Lf) resistance
Detailed measurements were made to establish which of these factors made a significant contribution to current imbalance between the modules. These showed that the imbalance was greater for lower values of pulsewidths. This is because the peak transistor current is dominated by the resonant currents of the snubber circuit at low pulsewidths and these currents will vary between the two modules by the tolerances of the snubber circuit components.

Current sharing was significantly improved by the insertion of a low resistance in each module output. Strips of stainless steel of various widths and lengths were connected between the modules – Figure 5.38a. The output was tapped along the strip (in holes punched at 20mm intervals). Using this technique, balance between the modules under static load conditions was achieved over a wide range of currents (Figure 5.38b). A 350mm x 45mm strip produced the best results with a maximum imbalance @ 350A of less than 10A under load and short circuit conditions. This indicated that the current between the modules is influenced primarily by the output resistance of each module (Vce(sat), Lf, Vf resistances). Dynamic current sharing is dominated by the snubber components and circuit inductances and are more difficult to equalise.

5.7.2 Output Waveforms

Iref was pulsed between 50A and 400A and the current waveforms produced recorded. All tests were on a load
resistance of 0.04 ohms. Figure 5.39 shows load waveforms measured at an output current of 450A. In P37, the 300Hz ripple current is due to the inability of the control system to fully attenuate mains rectified frequency. P38 shows a 30kHz ripple due to the bi-phase operation. In P34, P35, P36 (Figure 5.39), the rising edge of the pulse shows an initial \( \frac{d(iL)}{dt} \) of 200A/ms as the circuit is operating at the maximum pulsewidth (55μs, 15kHz). As the current error decreases, the control system reduces the pulsewidth, resulting in a lower \( \frac{d(iL)}{dt} \) and higher ripple. Pulse rise and fall times of 2.5ms and 4.0ms respectively were measured. These are much longer than predicted by the computer model and is due to the inductance of the load bank which varies between 50 - 250μH, depending on the load resistance selected.

5.8 Conclusions

The practical results have demonstrated the feasibility of designing a 250A transistorised chopper with a 15kHz modulating frequency. By paralleling two such modules, a 450A output current was obtained. Current sharing between the modules was controlled to within ± 10A under static conditions only. Ripple current amplitudes of less than 3.2A were achieved when the power modules were connected in parallel.
Waveform sketches showing method of output current ripple amplitude reduction

--- phase A
- phase B

control circuit ramps

pulsewidths (@25%)
pulsewidths (@50%)
pulsewidths (@75%)

current ripple at 25% pulsewidth
current ripple at 50% pulsewidth
current ripple at 75% pulsewidth

Phase A = module 1
Phase B = module 2

Schematic of two power modules connected in bi-phase mode (parallel operation)

FIGURE 5.36
<table>
<thead>
<tr>
<th>Iref (A)</th>
<th>i1 (PM1)</th>
<th>i2 (PM2)</th>
<th>i (11-12)</th>
<th>Ripple p/p</th>
<th>i1</th>
<th>i2</th>
<th>Io</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>25.3</td>
<td>24.6</td>
<td>+0.70</td>
<td>20</td>
<td>20</td>
<td>3.2</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>50.9</td>
<td>50.2</td>
<td>+0.62</td>
<td>20</td>
<td>20</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>99.2</td>
<td>102.2</td>
<td>-3.00</td>
<td>20</td>
<td>20</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>159.2</td>
<td>142.2</td>
<td>+17.00</td>
<td>20</td>
<td>20</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>350</td>
<td>175.2</td>
<td>178.5</td>
<td>-3.30</td>
<td>20</td>
<td>20</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>400</td>
<td>199.5</td>
<td>204.8</td>
<td>-5.30</td>
<td>20</td>
<td>20</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>450</td>
<td>226.4</td>
<td>227.4</td>
<td>-1.00</td>
<td>20</td>
<td>20</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>500</td>
<td>222.1</td>
<td>233.1</td>
<td>-11.00</td>
<td>20</td>
<td>20</td>
<td>2.0</td>
<td></td>
</tr>
</tbody>
</table>

i1 = PM1 output current  
i2 = PM2 output current  
Io = total output current (i1 + i2)

Current Sharing between Power Modules

FIGURE 5.37
View of power source showing two power modules with their outputs connected through the tapped resistor.

Figure 5.38a
<table>
<thead>
<tr>
<th>Iref</th>
<th>11 (PM1)</th>
<th>12 (PM2)</th>
<th>i (11-12)</th>
<th>11 (11-12)</th>
<th>12 (11-12)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>24.0</td>
<td>26.0</td>
<td>-2.0</td>
<td>25.2</td>
<td>28.0</td>
</tr>
<tr>
<td>100</td>
<td>46.8</td>
<td>54.4</td>
<td>-7.6</td>
<td>50.4</td>
<td>52.4</td>
</tr>
<tr>
<td>150</td>
<td>69.2</td>
<td>84.0</td>
<td>-14.8</td>
<td>74.4</td>
<td>77.2</td>
</tr>
<tr>
<td>200</td>
<td>95.6</td>
<td>109.6</td>
<td>-14.0</td>
<td>98.0</td>
<td>104.4</td>
</tr>
<tr>
<td>250</td>
<td>116.0</td>
<td>137.2</td>
<td>-21.2</td>
<td>130.0</td>
<td>126.0</td>
</tr>
<tr>
<td>300</td>
<td>142.0</td>
<td>164.0</td>
<td>-22.0</td>
<td>154.4</td>
<td>153.6</td>
</tr>
<tr>
<td>350</td>
<td>173.6</td>
<td>184.4</td>
<td>-10.8</td>
<td>185.2</td>
<td>175.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output from top hole of sharing resistor</th>
<th>Output from centre of sharing resistor</th>
</tr>
</thead>
</table>

Current Sharing with/without Balancing Resistor

FIGURE 5.38b
Load current waveforms for two power modules (450A) connected in parallel

**P34**

- **iL 50A/div**
- **T.B. 1ms/div**

**P35**

- Pulse rise period
- **T.B. 0.5ms/div**

**P36**

- Pulse decay period
- **T.B. 0.5ms/div**

**P37**

- 2A/div
- **T.B. 1ms/div**
- 300Hz component

**P38**

- Ripple current
- **1A/div**
- **T.B. 20us/div**
- Ripple frequency
- **30 kHz**

FIGURE 5.39
6. A 450 AMPERE MIG POWER SOURCE BASED ON THE 15kHz TRANSISTOR CHOPPER PRINCIPLE

6.0 Introduction

The power modules were used to develop a MIG power source capable of providing the specification outlined in Chapter 3. This Chapter describes the design and performance of the power source.

6.1 Power Source Description

The schematic of Figure 6.1 shows the general layout of the various subassemblies that constitute the MIG Power Source.

The 3Ø supply is fused and then connected to the welding transformer (TX1) via an isolating contactor. The primary of TX1 has voltage taps for 380, 420 and 440V rms supplies. The electronics and wirefeeder supply transformers (TX2, TX3 respectively) are connected via individual fuses to two phases of the mains supply. The fan motor operates from a 240V rms supply and is connected between the star point of TX1 and one of the incoming phases. The secondary windings of TX1 are isolated from the primary for operator safety reasons. The secondary is delta wound in order to reduce the flow of third harmonic currents in the windings. The secondary voltage is rectified by the 3-phase diode bridge (DB1) which is rated for 500A average current. An electrolytic capacitor bank (120,000 uF, 63V, 500A rms) provides a low impedance source for the switching currents drawn by the power modules. The rectified output is at 65V potential.
open circuit) and has a droop of 1.5V/100A when loaded. Three electronic cards perform the functions of machine/operator interface (Sequence Card), welding process control (Process Card) and output power control (PWM Card).

6.1.1 Sequence Card

The sequence card (Figure 6.2) performs the following functions:
- detects an over-temperature condition (via thermal switches) on the power module and diode bridge heatsinks (de-energises relay RL1)
- detects loss of supply on any of the electronic cards and inhibits machine operation via relay RL2
- energises relay RL4 and RL9 when the weld start signal is received from the operator
- activates the 3Ø contactor if RL1,2,4,9 are energised; the power modules are enabled by an auxiliary contact on the main contactor
- generates a 24V d.c. supply for the relays and lamps

6.1.2 Pulse Width Modulation (PWM) Card

The PWM card accepts a ± 10V signal from the current control error amplifier, on the process card, and converts these into digital pulses of variable pulsewidth and frequency. These signals are buffered and connected to pulse transformers which provide the electronic isolation between the control and power stages of the machine. The pulse transformer outputs are connected to the input stages of the Base Drive card. The control strategy described in Section 4.4.3
demands a constant frequency, variable pulselength (CFVP) for conditions when the load current (iL) is less than the current reference (Iref). If iL is greater than Iref, the pulse-width is reduced to its minimum (5.0μS), and the frequency is varied to maintain regulation. The output from IC10/1 (Figure 6.3) is at + 10V for the CFVP mode causing IC1 to produce a 30kHz pulse train into IC4. The Q and Q̅ outputs of IC4 are the bi-phase clocks (15kHz) for the two power modules. These clocks are used to drive the ramp generators (TR2, C29; TR3, C30). The ramps and the current error signal are compared at IC6,7 to produce PWM signals which are buffered and fed to the pulse transformers. The minimum pulselength is set by VR3 and maximum pulselength by VR1 (VR4). In the CFVP mode, the frequency is constant at 15kHz and the pulselength varies between 5.0 - 55μS. In the VFCP mode, the pulselength is set to 5.0μS and the frequency varies between 500Hz and 15kHz.

6.1.3 Process Control Card

The status of the machine output is determined by the truth table of Figure 6.4a. In the absence of a weld instruction from the operator, the power modules are inhibited (on the Base Drive Card). When a weld instruction is received (SEQ/RL4, 9), the power modules and the wirefeeder are enabled simultaneously. When the wire touches the workpiece (connected to the output -ve terminal) the power source output is shortcircuited and a shortcircuit current (Isc) flows and melts the wire tip. When the resulting
arc voltage is greater than 10V, the current reference
switches to Iref. The current reference toggles between
Isc/c and Iref and this is controlled by the steering
circuits (IC18c, IC19a, Figure 6.4b), as per the truth

table for output control.
The output current is measured using a d.c. current
transformer (DCCT/300) which produces an isolated
signal of 0 - 5V d.c., for a 0 - 500A current flowing
through it. IC15, IC17 process the DCCT signal prior
to it being connected to the error amplifier (IC8) and
metering circuit (IC26). An overcurrent condition
(iL > 500A) is detected by comparator (IC16) and its
output overrides the feedback signal at IC8, causing
the error signal to go positive (minimum pulsewidth,
VFCP mode).
The output voltage is measured by a d.c. voltage
transformer (DCVT/1000) connected across the output
terminals. It produces a 0 - 5V d.c. signal for a
0 - 50V output.

Synergic Pulse Current Generator
When the Pulsed Current MIG process is selected by the
operator, Iref is a d.c. pulsed current which is
required to follow the equation
\[
Im = \frac{Ip.Tp + Ib.Tb}{(Tp + Tb)} \\
\]

where Im is the average welding current.
The circuit also determines the wirefeed rate
required to give a constant arc length for a given
Im. Im is set by the operator. This signal is fed to
<table>
<thead>
<tr>
<th>Weld Status</th>
<th>iL</th>
<th>VL</th>
<th>Iref</th>
<th>Isc</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>non-welding</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>o/c volts</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>s/c volts</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>s/c current</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>weld @ Iref</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>weld @ Isc</td>
</tr>
</tbody>
</table>

Notes:

Weld Status 0 = non-welding condition
Weld Status 1 = welding condition

iL = 0; arc current < 50A
iL = 1; arc current > 50A
VL = 0; arc voltage < 10v
VL = 1; arc voltage > 10v
Iref = 0; arc current reference is Isc
Iref = 1; arc current reference is Iref
Isc = 0; arc current reference is Iref
Isc = 1; arc current reference is Isc

Truth Table showing power source output status

FIGURE 6.4a
the welding frequency (Fm) generator IC1. The Fm/Im ratio is determined by the gain of IC21. Three different gains are set corresponding to three welding programme channels. The welding programme select relays RL4 to RL9 are used to select values of Ip, Tp, Ib, Tb and wirefeed rates (metres/minute/100A) for each programme. Tp (peak pulse time) is generated at IC4 where a d.c. signal is compared with a ramp (IC10, C35). The ramp is reset by pulses from IC2. IC3 steers Ip to the current reference amplifier (IC6) during the Tp period (Ib during Tb). Ib is controlled by the averaging circuit R84, C57, IC7. As Im is varied, a pulse train is produced which has constant Ip, Tp parameters but with Ib, Tb varied to satisfy equation (98). The wirefeed rate is varied simultaneously to maintain a constant arc length. Typical pulse parameters for 1.0, 1.2 and 1.6mm diameter mild steel wires are given in Figure 6.5.

Arc Length Control

Conventional MIG power sources operate with a constant voltage characteristic i.e. the output voltage is maintained constant at its set value which in turn produces a constant arc length. Changes in arc length will occur when a constant current characteristic is used instead. The arc length can only be controlled by detecting this change in arc length (∝ to arc voltage) and altering either Im (burnoff more or less wire) or the wirefeed rate (feed more or less wire). If Im is altered, the power source can counteract a 1mm change in arc length in less than 5 ms. If the wirefeed
### Wire diameter: 1.0mm

<table>
<thead>
<tr>
<th>Im (A)</th>
<th>Ip (A)</th>
<th>Tp (ms)</th>
<th>Ib (A)</th>
<th>Tb (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>225</td>
<td>5</td>
<td>19.0</td>
<td>28.3</td>
</tr>
<tr>
<td>100</td>
<td>225</td>
<td>5</td>
<td>46.0</td>
<td>11.7</td>
</tr>
<tr>
<td>150</td>
<td>225</td>
<td>5</td>
<td>88.0</td>
<td>6.1</td>
</tr>
<tr>
<td>200</td>
<td>225</td>
<td>5</td>
<td>162.0</td>
<td>3.3</td>
</tr>
</tbody>
</table>

### Wire diameter: 1.2mm

<table>
<thead>
<tr>
<th>Im (A)</th>
<th>Ip (A)</th>
<th>Tp (ms)</th>
<th>Ib (A)</th>
<th>Tb (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>380</td>
<td>4</td>
<td>43.3</td>
<td>36.0</td>
</tr>
<tr>
<td>100</td>
<td>380</td>
<td>4</td>
<td>30.0</td>
<td>16.0</td>
</tr>
<tr>
<td>150</td>
<td>380</td>
<td>4</td>
<td>52.0</td>
<td>9.3</td>
</tr>
<tr>
<td>200</td>
<td>380</td>
<td>4</td>
<td>80.0</td>
<td>6.0</td>
</tr>
<tr>
<td>250</td>
<td>380</td>
<td>4</td>
<td>120.0</td>
<td>4.0</td>
</tr>
<tr>
<td>300</td>
<td>380</td>
<td>4</td>
<td>185.0</td>
<td>2.6</td>
</tr>
</tbody>
</table>

### Wire diameter: 1.6mm

<table>
<thead>
<tr>
<th>Im (A)</th>
<th>Ip (A)</th>
<th>Tp (ms)</th>
<th>Ib (A)</th>
<th>Tb (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>420</td>
<td>5</td>
<td>8.8</td>
<td>45.0</td>
</tr>
<tr>
<td>100</td>
<td>420</td>
<td>5</td>
<td>20.0</td>
<td>20.0</td>
</tr>
<tr>
<td>150</td>
<td>420</td>
<td>5</td>
<td>34.0</td>
<td>11.7</td>
</tr>
<tr>
<td>200</td>
<td>420</td>
<td>5</td>
<td>53.0</td>
<td>7.5</td>
</tr>
<tr>
<td>250</td>
<td>420</td>
<td>5</td>
<td>80.0</td>
<td>5.0</td>
</tr>
<tr>
<td>300</td>
<td>420</td>
<td>5</td>
<td>121.0</td>
<td>3.3</td>
</tr>
<tr>
<td>350</td>
<td>420</td>
<td>5</td>
<td>190.0</td>
<td>2.1</td>
</tr>
</tbody>
</table>

Shielding gas: Argon 95%, CO2 5%

N.B. Im is continuously variable between 50 and 350A

**Typical Pulse Parameters for Mild Steel Wires**  
(Pulsed MIG Process)

**FIGURE 6.5**
rate is altered instead, a similar change in arc length will be counteracted in 50 ms - due to the limited response of the wirefeeding motor/feed mechanism (> 250 ms) - Figure 6.6. The advantage of the wirefeed method, is that the welding current is constant under all operating conditions. This is a prime requirement for consistent fusion of the weld. A simple control loop (Figure 6.6) was therefore selected for arc length control using the variable wirefeed rate method. The reference for the loop is generated from the equation

\[ V_{ref} = 20 + 0.04 I_m \]

Vref varies with weld current to account for the higher voltage drops in the anode and cathode regions of the arc. Arc length is proportional to 20V and is constant over the full range of Im (50 - 350A). Vref is generated at IC22a with IC22b forming the error amplifier for the loop. The output of IC22b biases TR3 (FET) for linear operation between full conduction and cutoff. TR3 is used as a variable resistor to give between 30% and 70% of the wirefeed reference (Wref). This is added to a signal equal to -50% of Wref to produce ±20% of Wref at IC23a. This trim signal is summed with Wref at IC12b whose output becomes the reference signal for the wirefeeder motor control circuit.

Dip Transfer Control - reference Figure 6.7

In the Dip Transfer mode, Iref is generated by arc conditions as opposed to being preset. Wref is set by the operator and the circuit determines Isc, Tsc and
CONTROLLED DIP TRANSFER
CIRCUIT DIAGRAM
FIGURE 6.7
Iarc. Isc is fixed for all wire diameters at 450A.

When a short circuit is detected (IC1a), delay circuit (IC6a) is enabled. When monostable IC4 times out, the current reference is switched to Isc.

When the arc ruptures, IC1 detects the voltage change and switches Iref from Isc to Iarc at IC10a. As the wirefeed rate is greater than the wire burnoff rate, the wire will repetitively short to the weld pool.

\( \frac{d(iL)}{dt} \) is controlled by slew rate capacitors across IC10a. These are switched into circuit by IC11 and IC9.

The Dip Transfer current reference is connected to the process card error amplifier (IC8). During the Dip Transfer mode, the Iref used for Pulsed operation is disabled by Dip Relay RL2, RL3 (Figure 6.4b).

6.2 Power Source Electrical Performance

Initial welding tests on the machine were carried out with a 1.2mm mild steel (LW1) wire in "Argoshield 5" shielding gas. Under these conditions, several tests were performed to determine the electrical performance of the machine.

6.2.1 Load Current Waveforms - Pulsed Iref

A typical current waveform taken under welding conditions is given in Figure 6.8a.

Pulse rise (tR) and fall (tF) time measurements are given in Figure 6.8b for constant peak parameters but varying background currents. These show that rise and fall times of 1.0 ms and 1.5 ms respectively are obtained under arc load conditions (c.c.2.5, 4.0 ms respectively on a resistive load - Section 5.6).
6.2.2 Power Bandwidth (Fp) Measurement

Using the set up of Figure 6.9, a Transfer Function Analyser (TFA) was used to measure the frequency response of the machine under closed loop conditions. A 0.1V p/p sinewave signal was fed into the current amplifier (IC8, Process Card) and superimposed on Iref. The wirefeed rate was adjusted to give an arc length of approximately 5mm. The torch was mounted on a horizontal traverse mechanism and bead-on-plate welds placed on a 12mm thick mild steel plate (to minimise plate distortion). The measurements were therefore made with an approximately constant arc length. The 3dB point occurs at 380Hz (Figure 6.9).

6.2.3 Efficiency Measurement

Efficiency tests were carried out on an arc load with a pulsed Iref. The welding current (Im) was varied from 50 - 350A and input/output power measured. The plot of Figure 6.10 shows that optimum power source performance occurs above Iref = 200A. The losses in the transformer (iron), Base Drive circuits, fan motor etc are constant over the full power range and will therefore decrease machine efficiency at lower power outputs.

6.2.4 Output Characteristics Plot

The machine operates with a constant current characteristic (100% current feedback). By varying the load resistance (1.0Ω → 0.1 mΩ), for different values of Iref (100, 200, 300, 400A), the machine regulation has been plotted – Figure 6.11. This is better than
5A/50V. De-regulation occurs at high load resistance values because the maximum pulsewidth has been restricted to 55μs, thus preventing the power module from generating output voltages greater than 45V under load conditions. The de-regulation at low voltages (< 1V) occurs because the PWM circuit is unable to reduce the frequency (below 500Hz) in accordance with equation (72) (VFCP operation). This minimum frequency is limited by the V/F converter, (IC1 Figure 6.3) which has a range of 50:1 (600Hz - 30kHz) only. A converter with a 100:1 range is required to improve the regulation at low output voltages.

6.2.5 Electrical Conducted Noise

Measurements of conducted interference emissions were made for comparison with the VDE 0871 Class A specification and to American FCC Rules Part 15 Sub Part I Class A specification.

For all measurements, the power source was operated with an arc load. The layout and measuring equipment and operating conditions are shown in Figure 6.12a.

Measurements were carried out by ERA Technology, and the following results are a summary of their report.

Conducted Interference

Mains Terminal Voltage: 10 kHz - 150 kHz

Measurements of conducted interference were made over the stated frequency range using a Schwarzbeck LSME 1530 radio interference measuring receiver in conjunction with a three phase line impedance stabilising network (LISN). The receiver has a normal
bandwidth of 200kHz, quasi-peak pulse response and complies with the requirements of CISPR Publication No 16 and VDDE 0876.

Mains Terminal Voltage: 0.15MHz - 30MHz

Measurements of conducted emissions were made using a Chase Electrics HFR 2000 radio interference measuring receiver in conjunction with a three phase LISN. The receiver has a normal bandwidth of 9kHz, a quasi-peak pulse response and complies with CISPR Publication No 16, ANSI C63.2 and VDE 0876.

Results

Mains Terminal Voltage: 10kHz - 30MHz

The results of the conducted interference measurements are given in Figure 6.12b. The highest recorded signal level (dBuV) was greater than 120 dB, at 30kHz measuring frequency. The arc current was set at 275A d.c. continuous and also at two pulsed current levels.

Conclusions

The maximum reading of 120 dB was obtained at 30kHz. This corresponds to the bi-phase output modulating frequency at which the two power modules draw power from the mains supply. Readings of 91dB (@ 15kHz) and 103dB (@ 60kHz) produced the only other measurements above 90 dB. The readings indicate that the power source does NOT comply with the VDE 0871 Class A or FCC Class A recommendations.

Line noise suppression, giving a 40dB attenuation for frequencies less than 2MHz, is required.
Typical pulsed current waveform into an arc load

**FIGURE 6.8a**

<table>
<thead>
<tr>
<th>Ib</th>
<th>tR</th>
<th>tF</th>
<th>Im</th>
<th>Vm</th>
<th>Wire Speed (m/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A)</td>
<td>----ms----</td>
<td>(A)</td>
<td>(V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>1.0</td>
<td>1.0</td>
<td>216</td>
<td>26</td>
<td>5.5</td>
</tr>
<tr>
<td>100</td>
<td>1.0</td>
<td>1.0</td>
<td>242</td>
<td>27</td>
<td>6.3</td>
</tr>
<tr>
<td>150</td>
<td>0.9</td>
<td>1.5</td>
<td>255</td>
<td>30</td>
<td>6.5</td>
</tr>
<tr>
<td>200</td>
<td>1.0</td>
<td>1.5</td>
<td>265</td>
<td>34</td>
<td>6.7</td>
</tr>
</tbody>
</table>

Conditions:
- Gas: Ar 95% CO2 5%
- Ip: 400A
- Tp: 5ms

Pulse current rise/fall time measurements under arcing conditions and for different background currents

**FIGURE 6.8b**
Schematic of frequency response measuring equipment

3dB point (380 Hz)

Frequency response curve of 450A power source

FIGURE 6.9
Power source efficiency plot

FIGURE 6.10

- Maximum welding current
- Minimum welding current

**Measurements into an arc load**
- 1.2mm mild steel wire
- Ar 95%, CO2 5% gas
- 5mm arc length
- Pulse current mode

**Welding current - Amperes**
**Efficiency - %**
Power Source output current regulation curves

FIGURE 6.11

Load resistance varied from 1 ohm to a short circuit (.01 ohm)

Output voltage - volts

Iref = 100A  Iref = 200A  Iref = 300A  Iref = 400 A

Output current - Amperes

start of deregulation
Test conditions for the electrical conducted noise measurements

Current (Amperes)

<table>
<thead>
<tr>
<th>3Ø mains + Earth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power source</td>
</tr>
<tr>
<td>3Ø LISN</td>
</tr>
<tr>
<td>Measuring receiver 1530/HFR 2000</td>
</tr>
</tbody>
</table>

Layout of measuring equipment

Current (Amperes)

2m 3m

d.c. pulsed
Iaverage 350A

280

Time

Current (Amperes)

380

380

d.c. pulsed
Iaverage 105A

19m

50

Time

FIGURE 6.12a
Narrowband Noise Ø
Broadband Noise ø-ø

Maximum Measurable Signal Level
Po = 15 kHz

Electrical noise (conducted) plotted for 350A pulsed condition

FCC Class A Limits
VDE 0871 Class A

M450 PS Welding Source, (d.c level = 275A)

FIGURE 6.12b

Mains Terminal Voltage
6.3 Acoustic Arc Noise Measurements

The Pulsed Current MIG Process produces considerable acoustic noise compared to conventional MIG Spray Transfer Processes. The welding arc has a bandwidth greater than 100kHz and is capable of reproducing the entire frequency spectra of audible noise in the arc. The acoustic noise is produced by the modulation of the shielding gases that form the arc. These set up sound pressure waves at the welding frequency (50 - 300Hz) and the modulating frequency (15kHz, 30kHz).

The tests were carried out by the Open University. Comparisons with a series linear regulator and a transistorised chopper power source (Fo = 2kHz) were also performed.

Method

A calibrated tape recording was made of the background level in the test area and the arc noise for each operating condition (for each power source). The welding torch was connected to an automatic traverse rig that produced a linear weld one metre long per test run. Calibration was effected using a Pistonphone producing 124 db (linear) when close coupled to a microphone. During each operating cycle, a tape recording was made through a sound level meter which enabled monitoring of the levels being recorded. Independent readings of the "A weighted" equivalent sound level (LAeq) were made using an integrated sound level meter. The relative positions of the measuring equipment are
shown in Figure 6.13a. The recording position was approximately 0.5m from the welding track.

Results

a) The noise measurement during the short circuit period at the start of the weld is shown in Figure 6.13b. Peak values exceed 100 dbA.

b) Recordings during the weld cycle were performed with a continuous d.c. current spray arc and pulsed currents up to 350A. Figure 6.14a shows a typical plot over the full spectra. A prominent, clear tone at 15kHz (88db) is present (the power source modulating frequency).

c) The broad band and narrow band results for the three different types of power sources showed that the low frequency chopper set (LFC) consistently produce higher "A" weighted noise levels. This is due to the larger energy contribution above 2kHz. The series linear regulator sets (SLR) produces more energy, between 200Hz - 1kHz. The high frequency chopper (HFC) power source produces noise consistently below 84dbA at all current levels. From Figure 6.14b, the HFC power source is marginally noisier than the series linear regulator set. The LFC set produces the highest noise levels (88.3dbA).

6.4 Arc Instabilities

The power source current control system will deregulate if the arc impedance, arc current product is greater than the chopper supply voltage (Vi). Transient deregulation of the arc current can therefore occur.
Acoustic noise measurement - operating into an Arc load

FIGURE 6.13a

Brüel & Kjær

Noise levels dB

95
90
85
80

Paper speed 3mm/second

Noise measurement for consecutive short circuits at the start of a weld

FIGURE 6.13b
Traces of the acoustic noise emitted by the arc when using the HFC Power Source

FIGURE 6.14a
<table>
<thead>
<tr>
<th>Welding current (A)</th>
<th>Power Source Type</th>
<th>Noise level dbA</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>Mitsubishi (LFC)</td>
<td>87.2</td>
</tr>
<tr>
<td>150</td>
<td>Mitsubishi (LFC)</td>
<td>88.3</td>
</tr>
<tr>
<td>150</td>
<td>M450 (HFC)</td>
<td>83.3</td>
</tr>
<tr>
<td>250</td>
<td>M450 (HFC)</td>
<td>81.7</td>
</tr>
<tr>
<td>300</td>
<td>M450 (HFC)</td>
<td>83.0</td>
</tr>
<tr>
<td>350</td>
<td>M450 (HFC)</td>
<td>79.7</td>
</tr>
<tr>
<td>300</td>
<td>M500 (SLR)</td>
<td>83.0</td>
</tr>
<tr>
<td>350</td>
<td>M500 (SLR)</td>
<td>78.7</td>
</tr>
</tbody>
</table>

Acoustic arc noise comparison between power sources of different technologies

FIGURE 6.14b
since the arc has a higher bandwidth than the power source. If the power source deregulates, the arc current is reduced to zero and the arc extinguishes. If this occurs regularly during a welding cycle, then the arc is considered to be unstable. Three different but related forms of arc instabilities have been identified in the welding tests performed. These are observations not previously reported by other authors.

6.4.1 Current Undershoot Instability

With a normally running Pulsed Current MIG arc, an occasional "popping" sound was heard without any sign of wire-weldpool short-circuiting occurring. This was observed over the full range of welding currents (60 – 350A) and with all combinations of wire compositions and sizes. Examination of arc current and arc voltage traces revealed the presence of arc outages during the falling edge of the current pulse - Figure 6.15. The power source supply voltage, which is limited to 65V, maintains gas ionisation and the arc recovery occurs naturally. With series linear regulator types of power sources, the arc impedance changes are absorbed by an equivalent change in the impedance of the transistors - statically and dynamically. With chopper types of power sources, the filter inductor, \( L_f \), buffers the load from the transistors. Any change in arc impedance is therefore counteracted only after a delay proportional to the power source response (\( \alpha L_f F_o \)) which results in transient arc outages. This form of instability was avoided by slew
rate limiting the reference current on the falling edge. This has the effect of reducing the rate of change of arc impedance (Δi/Δt arc current) and consequently preventing arc instabilities. As shown in Figure 6.15c, the current control loop was able to follow and regulate against arc impedance changes. The absence of the current undershoot indicates a stable arc. The "popping" sound previously present during a weld was also found to be absent.

6.4.2 Low Background Current Induced Instability

In Pulsed Current MIG operation, background currents below 50A produce more severe forms of arc instabilities - Figure 6.16 where a complete cycle of current is absent. The progressive increase in arc impedance is observed in the transition from normal operation (pulse No 1,2,3) to falling edge instability (Pulse No 4,5) to complete background instability (Pulse No 6) after which a pulse of current is absent. During arc outages, the power source terminal voltage is at the open circuit value (65V), suggesting that the arc is at a very high impedance (arc extinguished). The recovery of the arc occurs naturally (i.e. the wire does not strike the weld pool). This is probably because the ionisation potential of the gases is low (as the cathode and anode of the arc are still hot). The open circuit voltage is sufficient to reionise the gases under these conditions.

6.4.3 Low Background Voltage Induced Arc Instability

Arc instability due to the depression of the background arc voltage is caused by a reduction in the arc length.
In constant current welding, this can occur for a number of reasons:

- for a fixed torch-workpiece separation, fluctuating wirefeeding can cause arc length changes (Figure 6.17a), which results in the wire shortcircuiting to the weldpool (arc extinguishes).

- for a constant wirefeed rate, a reduction in torch-workpiece separation will produce a similar effect (Figure 6.17b); this has been observed when the arc is weaved across a V-shaped weld joint (Figure 6.17c); the arc length is suppressed at the walls of the joint (A,A') causing arc outages.

- remnant magnetism in the workpiece can cause arc deflection as a result of the interaction of the arc electric fields and the workpiece magnetic fields, causing the arc to extinguish.

The arc instabilities are characterised by the loss of complete cycles of weld current and intermittent shortcircuiting of the wire to the weld pool. The arc length decreases with each pulse of current that is missing. Eventually, the wire strikes the weld pool causing a shortcircuit current to flow and re-establish the arc. A trace taken in a vertical up (V-joint) weld with side to side oscillation of the torch produces the instabilities at the extremeties (A,A') of the weld joint only - Figure 6.18a. The
Arc instability due to current undershoot

Arc current 50A/div
T.B. 10ms/div
load: welding arc
FIGURE 6.15a

Arc current
T.B. 2ms/div
expanded pulse
to show undershoot
FIGURE 6.15b

current reference
with slew rate
limited falling edge

Arc current
100A/div
T.B. 2ms/div
current undershoot
absent
FIGURE 6.15c
Arc instability during the current background period and the falling edge of the pulse

Arc current
50A/div
T.B. 10ms/div

open circuit voltage

Power Source terminal voltage
20v/div: T.B. 20ms/div

voltage (arc) during instability

Power Source terminal voltage for a normal running arc
10v/div
T.B. 5ms/div

FIGURE 6.16
Arc instability due to arc length depression

Arc length depression due to a fluctuating wirefeed rate - @ constant arc current

Arc length depression due to a decreased torch-workpiece separation - @ constant arc current

Torch movement

Arc length varies as the torch weaves across the weld joint (unstable arc at A, A')

Arc voltage control system varies wire stickout to give a constant arc length as the torch weaves across the weld joint (stable arc)

FIGURE 6.17
Arc current traces taken during a vertical-up positional weld in a 120° weld preparation.

**FIGURE 6.18a**

- Arc instability at A
- Stable arc
- Arc instability at A'

AVC system switched off

**FIGURE 6.18b**

- Minor arc instability at A
- Stable arc
- Minor arc instability at A'

AVC system used to stabilise arc length
instabilities do not occur if the torch-workpiece separation (standoff) is increased at the side walls of the joint. An arc voltage control (AVC) system was used to automatically adjust the standoff. Background voltage instabilities could therefore be minimised by automatically limiting the arc length to values giving stable arcs - Figure 6.18b.

6.5 Power Source Welding Performance

(summarised data in Appendix C )

The Pulsed Current and Dip Transfer Process performance of the power source below is a summary of the work 52,53 carried out by the Cranfield Institute of Technology. The purpose of these tests was to verify the performance of the high frequency chopper based power source in the Pulsed Current and Dip Transfer modes.

6.5.1 Dip Transfer

The use of constant current characteristic power source for Dip Transfer has been restricted to research experimentation only. As described in Section 2.6.1, optimum Dip Transfer requires:

- low spatter of weld metal on the workpiece
- adequate fusion properties for all torch-workpiece separations
- a regular Dip frequency to produce a constant detachment of metal and smooth weld bead properties
- constant wire feed delivery
Experimental Procedure

All the tests were carried out using "Argoshield 5" gas and 0.8, 1.0, 1.2mm mild steel (LWl) wire.

Torch-workpiece distance was approximately 15mm.

The I_{sc} and V_{detect} levels were set at those producing optimum conditions. I_{arc} was then varied to give a stable welding condition. The inductance was then varied to reduce spatter levels and improve the bead profile.

A general trend was observed in the readings obtained:
- A relationship exists between wire feed speed (W_{fs}) and I_{arc} (Figure 6.19) which could be used to produce a simple, single parameter (W_{fs}) control of the Dip Process.
- Reducing the arc current results in peaky bead profiles, less wetting and loss of process stability.
- Excessive inductance produced globular type of metal transfer.
- Spatter was marginally influenced by inductance.
- Process stability and bead appearance is improved with increased inductance.
- A distinct increase in fusion area was observed when the arc current was increased (for a given W_{fs}, I_{sc}, V_{detect} and inductance).
- Increasing the inductance produced a general increase in fusion area but had a more profound effect on weld width, producing consistently flatter beads at the higher inductances.
Relationship between I_{arc} and Wirefeed rate for the controlled Dip transfer process

![Graph showing the relationship between Arc current (Amp) and Wirefeed rate (m/minute) for 1.0mm and 0.8mm mild steel wire.](FIGURE 6.19)
Dip transfer process waveforms for the transistorised chopper power source

*shows effect of Td

Arc current 50A/div
T.B. 2.5ms/div

Arc voltage 20v/div
T.B. 2.5ms/div

Dip transfer process waveforms for a conventional transformer-rectifier power source: BOC Transmig 350

Arc current
N.B. variation in current peaks and duration

Arc voltage

FIGURE 6.20
Dip Transfer Waveform

Figure 6.20 shows current and voltage waveforms of the controlled Dip Transfer Process. The delay in the application of the short circuit current is observed. This delay allows the wire tip to penetrate and melt inside the pool rather than at the surface, where the explosive effects of wire melting and fusing would create the commonly experienced spatter of weld metal. The waveform produced by the conventional Dip Transfer process is very similar to that shown for the constant current Dip Transfer. However, Isc and Iarc are not controlled, leading to higher levels of spatter and variable fusion properties.

6.5.2 Pulsed Current Spray Transfer

A detailed analysis of the Pulsed Current Spray Transfer Process was given in Chapter 2. The practical work concentrated on the development of suitable pulse parameters for three sizes of mild steel wires. Welding procedures were then developed to evaluate these for the downhand, overhead, vertical and horizontal welding positions. Qualitative assessments of fumage, spatter and weld bead appearance have also been made.

General Results

- Metal deposition varied from 1.5 - 1.7kg/hr per 100A of welding current (Im) for all wire diameters
- Spatter was completely absent when the one droplet per pulse condition was observed; multiple droplets per pulse produced slight spatter and excessive fumes
- Weld penetration was shown to increase for higher values of \( I_b \) (for a given \( I_m \)) and for higher values of \( I_m \).

- As a comparison with conventional MIG welding, welds were performed and sectioned; the Pulsed MIG welds showed greater root and side wall fusion under the same welding conditions.

- Welding performance with 'Argoshield 20' shielding gas (80%Ar - 20%CO\(_2\)) was less satisfactory. Spatter free welds were unobtainable. The droplets detached were large, approaching globular, and were projected less axially into the weld pool than with 'Argoshield 5' (95%AR - 5%CO\(_2\)). The use of a higher percentage of CO\(_2\) gas prevents spherical droplets from forming on the tip of the wire.

- The welding of Aluminium alloys revealed an electrical limitation of the control system that regulates the current in the power modules. The latter failed regularly when used on 1.6mm, 99% pure Aluminium wire. During the shortcircuit period, the output voltage of the power source attains levels as low as 0.5 volts, due to the low resistance of the Aluminium wire. It was shown (Figure 6.11) that the current control loop deregulates at low output voltages. For a reference value of 450A, the measured output currents during the short-circuit period are shown in Figure 6.21a.
Measurement of current amplitude during shortcircuit tests to determine cause of power module failures

\[ \text{current overshoot at start of shortcircuit} \]

\[ \text{shortcircuit current reference} \]

<table>
<thead>
<tr>
<th>Wire diameter / Wire composition</th>
<th>Isc (min)</th>
<th>Isc (max)</th>
<th>Isc (mean)</th>
<th>Sample size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2mm/99%Al</td>
<td>488</td>
<td>689</td>
<td>628</td>
<td>21</td>
</tr>
<tr>
<td>1.6mm/99%Al</td>
<td>577</td>
<td>689</td>
<td>650</td>
<td>21</td>
</tr>
<tr>
<td>1.2mm/mild steel</td>
<td>400</td>
<td>667</td>
<td>546</td>
<td>21</td>
</tr>
</tbody>
</table>

Results before control loop modification

FIGURE 6.21a

<table>
<thead>
<tr>
<th>Wire diameter / Wire composition</th>
<th>Isc (min)</th>
<th>Isc (max)</th>
<th>Isc (mean)</th>
<th>Sample size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2mm/99%Al</td>
<td>478</td>
<td>492</td>
<td>478</td>
<td>21</td>
</tr>
<tr>
<td>1.6mm/99%Al</td>
<td>450</td>
<td>506</td>
<td>502</td>
<td>21</td>
</tr>
<tr>
<td>1.2mm/mild steel</td>
<td>450</td>
<td>478</td>
<td>475</td>
<td>21</td>
</tr>
</tbody>
</table>

Results after control loop modification

FIGURE 6.21b

(Isc measured in Amperes) Isc set value - 450A
Current spikes exceeding 450A are observed. This was remedied by introducing an additional current limit loop that switched the power modules off directly - bypassing the control system. This reduced the current overshoot (Figure 6.21b).

6.6 Summary of Power Source Performance

The electrical results reported show close agreement (Figure 6.22) with the required specification.

The power source has been de-rated to 450A for thermal reasons. Furthermore, the presence of a current overshoot during the shortcircuit mode has placed further limitations to the maximum output current that can be obtained reliably.

The power source bandwidth (Fp) is restricted to 380 Hz by the slew-rate limiting circuitry. The latter are required to improve arc stability.

The electrical conducted noise does not meet the requirements of the VDE0871. However, the specification is not mandatory for industrial equipment.

The welding performance in the Pulsed Current and Dip Transfer modes exceeds that for conventional equipment. Low spatter, consistent fusion properties and the ability to produce high quality all positional welds by the pre-programming of weld parameters are a major advance in the field of MIG welding.
<table>
<thead>
<tr>
<th>Power Source Results</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open Circuit Voltage</td>
<td>67.5V</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>450A</td>
</tr>
<tr>
<td>Full Load Current</td>
<td>350A</td>
</tr>
<tr>
<td>Maximum Load Voltage</td>
<td>50V</td>
</tr>
<tr>
<td>Current Ripple</td>
<td>3 to 7.5A</td>
</tr>
<tr>
<td>Accuracy</td>
<td>Better than 5A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>58 - 71%</td>
</tr>
<tr>
<td>Power Factor</td>
<td>&gt; 0.8</td>
</tr>
<tr>
<td>Pulse Rise times (tR)</td>
<td>&lt; 1.0 m</td>
</tr>
<tr>
<td>Pulse Fall times (tF)</td>
<td>&lt; 1.5 m</td>
</tr>
<tr>
<td>Full Power Bandwidth (Fp)</td>
<td>380Hz</td>
</tr>
<tr>
<td>Regulation (constant current mode)</td>
<td>&lt; 5A/50V</td>
</tr>
<tr>
<td>Electrical Mains Conducted EMI</td>
<td>Out of Specification</td>
</tr>
<tr>
<td>Acoustic Noise</td>
<td>&lt; 81 dBA</td>
</tr>
<tr>
<td>Dimensions</td>
<td>390(H) X 620(W) X 840(D)</td>
</tr>
<tr>
<td>Weight</td>
<td>150kg</td>
</tr>
<tr>
<td>Cost: (incl wirefeeder)</td>
<td>£4500</td>
</tr>
</tbody>
</table>

**Process Capability**

**Pulse Transfer**

1.0, 1.2, 1.6mm mild steel | Argoshield 5, Argoshield only 5 and 20 |
1.0, 1.2, 1.6 stainless     | Argonox 1, Argonox 1 |
1.2, 1.6mm Aluminium(95%)   | Argon, Argon |

**Dip Transfer**

0.8, 1.0mm mild steel      | Argoshield 5,20 |

**Comparison of Performance x Specification**

**FIGURE 6.22**
7. DISCUSSION OF RESULTS

7.1 Comparison between predicted and actual results

The computer model of the transistor chopper was developed to:

- predict switching waveforms in the power circuit
- generate data relating to device ratings and passive component selection
- predict the performance of the power source into an arc load

7.1.1 Waveform Comparisons

A comparison of the transistor switching waveforms between those predicted and actually observed are given in Figure 7.1, 7.2. The amplitudes and time scales are different as the two sets of results being compared are under different conditions. The transistor switching waveforms of Figure 7.1 show close agreement for the turn-on and turn-off periods.

The pertinent features of the waveforms are:

- the transistor current is $di/dt$ limited by $L_c$ at the start of the cycle (Figure 7.1c)
- it shows an overshoot of current, at turn-on, corresponding to the flow of $D_f$ reverse recovery current (Figure 7.2b)
- the snubber capacitor discharge current ($I_S$) flows in the transistor in the first few microseconds of the cycle (Figure 7.1b)
- a rapid increase in $V_{ce}$ occurs during the current fall time (Figure 7.1d)
Comparison between actual and predicted circuit waveforms

**FIGURE 7.1**

**Actual**

Transistor waveforms

Snubber current

Transistor turn on waveforms

Transistor turn off waveforms

**Model Predictions**

(a) Vce 50v/div 10us/div

(b) Vce 40A/div 10us/div

(c) Vce 50v/div 2us/div

(d) Vce 80A/div 1us/div
Comparison between actual and predicted circuit waveforms

**Actual**

50A/div

Vce 25v/div

**Predicted**

SOAR PLOT FOR 250A LOAD

Transistor Safe Operating Area

**FIGURE 7.2a**

Actual

Predicted

40A/div

40A/div

5us/div

Flywheel diode current waveforms

**FIGURE 7.2b**
7.1.2 Data Comparisons

More detailed data comparisons are made with reference to Figure 7.3 for operation at an Iref of 250A. The peak transistor current varies from 280 - 298A compared to a predicted 343A. For a given load and supply voltage, iT(peak) will vary between modules as a function of Lc, Qrr (of Df), Lf and the snubber circuit component tolerances. The model, therefore, was provided with the 'worst case' data which has produced a more pessimistic result compared to that actually obtained.

The Vce during the fall time (Tf), varies between 60 and 130V (130V predicted). This variation is due to the spread in the transistor turn-off times and circuit stray inductance values.

7.1.3 Error analysis

Measurement Errors

A number of factors influence the accuracy of the measurements of time, voltage and currents. As all readings were taken off an oscilloscope, the best resolution was ± 5% for all readings. Current measurements were subject to an error of ± 10% to account for the saturation of the current measuring probe at currents exceeding 250A.

Circuit Components Tolerance

Tolerances of circuit parameters are listed below:

- Supply Voltage : Vi ± 10%
- Inductances : Lc, Lf, Ls ± 20%
<table>
<thead>
<tr>
<th>Power Module No.</th>
<th>No.</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>Average</th>
<th>Model Results</th>
<th>Error %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Width-u</td>
<td>1</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td>56.0</td>
<td></td>
</tr>
<tr>
<td>Tr (u)</td>
<td>2</td>
<td>6.0</td>
<td>5.5</td>
<td>8.0</td>
<td>8.0</td>
<td>6.9</td>
<td>3.2</td>
</tr>
<tr>
<td>iT(Tr) (A)</td>
<td>3</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>343</td>
</tr>
<tr>
<td>Vce(sat) (V)</td>
<td>4</td>
<td>2.5</td>
<td>3.0</td>
<td>1.3</td>
<td>1.25</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>iT(Tf) (A)</td>
<td>5</td>
<td>180</td>
<td>200</td>
<td>200</td>
<td>184</td>
<td>191</td>
<td>256</td>
</tr>
<tr>
<td>Vce(Tf) (V)</td>
<td>6</td>
<td>70</td>
<td>60</td>
<td>60</td>
<td>130</td>
<td>80</td>
<td>130</td>
</tr>
<tr>
<td>Vce(pk) (V)</td>
<td>7</td>
<td>140</td>
<td>140</td>
<td>165</td>
<td>145</td>
<td>147</td>
<td>187</td>
</tr>
<tr>
<td>TC1</td>
<td>8</td>
<td>72</td>
<td>67</td>
<td>48</td>
<td>51</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>TC2</td>
<td>9</td>
<td>71</td>
<td>60</td>
<td>82</td>
<td>51</td>
<td>63.5</td>
<td>51.3</td>
</tr>
<tr>
<td>TC3</td>
<td>10</td>
<td>76</td>
<td>67</td>
<td>54</td>
<td>63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tf (u)</td>
<td>11</td>
<td>1.5</td>
<td>1.0</td>
<td>2.0</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0d C</td>
<td>12</td>
<td>62</td>
<td>41</td>
<td>46</td>
<td>54</td>
<td>146</td>
<td></td>
</tr>
<tr>
<td>Tamb C</td>
<td>13</td>
<td>22.5</td>
<td>23</td>
<td>21.0</td>
<td>20.0</td>
<td>33</td>
<td></td>
</tr>
</tbody>
</table>

Transistor type: <-ESM1000-> <-ESM3001->

No. off : 3 3

TC1,TC2,TC3 = transistor case temperature (°C)

0d = Df case temperature; Fo = 15kHz

Error = (Model - Actual)/(average of actual)

Model vs actual data comparison for Power Modules No. 1-4 @ Iref = 250A

FIGURE 7.3
Ambient Temperature : $\pm$ 5°C
Stray Inductances : $L_{xe}, L_{xf}, L_{xs} \pm 100$
Resistance : $R_L, R_s, R_c \pm 10$

The transistor and flywheel diode data used in the model represent typical values only. As no pre-selection of devices was carried out, differences can be expected between the predicted and actual results obtained for switching times, saturation voltages, $D_f$ recovered charge etc. A more detailed correlation of actual and predicted data has therefore not been presented. However, the model results are in all cases more pessimistic than the average of the actual results for most of the parameters measured (Figure 7.3b).

7.2 Transistor switching
7.2.1 Turn-on performance
The transistor does not fully saturate immediately for two reasons:
a) for a period of 5 - 10µs after being turned on, the transistor goes through a phase of dynamic quasi-saturation whilst the charges injected at the base-emitter junction begin to reduce the collector (N-) resistance
b) the flywheel diode ($D_f$) is in its reverse recovery mode and holds the emitter terminal of the transistor close to the negative supply potential - the device hence supports the full supply voltage

7.2.2 Turn-off performance
The effectiveness of the dynamic de-saturation of the transistor prior to applying reverse bias was
demonstrated in Section 5.5.4. This method reduced storage time and recovered charge and gave faster collector current fall times (< 1.5 μs @ 250A). However, decreasing Tf results in a higher voltage across the transistor during the fall time. The Vce during this period varies between 60 - 130V for an Iref of 250A. The corresponding d(IT)/dt is 120 - 184A/μs, which yield snubber circuit stray inductance values of between 0.58 - 0.71μH. The latter could be reduced by:

- providing individual snubber networks for each output transistor; these could be mounted near to each device to reduce the length (hence inductance) of the interconnecting cables; this method suffers from the drawback of complexity and cost
- by using a single snubber network, low inductance 66 cabling techniques could be used to reduce the stray inductance to less than 0.1μH; furthermore, the self inductance of Cs could be reduced by paralleling a number of small capacitors rather than using a single capacitor

7.2.3 Effect of collector circuit inductance (Lc) on Transistor dissipation

After the fall time period, Cs continues to be charged from the energy stored in Lc. This has the effect of increasing transistor Vce to between 140 - 165V (for V1 = 60V). The transistors are rated at a Vceo > 200V and can safely withstand this voltage. Cs is charged to the higher voltage levels, and the
subsequent discharge of Cs, at turn-on, produces
high currents in the transistors. A reduction in Vce(pk)
is therefore desirable and this can only be achieved by
reducing Lc. Tests were carried out for Iref up to 150A
to investigate the difference in turn-on losses,
transistor peak current and off-state voltage (Vce)
with and without Lc. The results are given in Figure 7.4
and these show that:
- iT(peak) is lower for Lc = 0.1uH, contrary to the
  original design expectations.
- Vce(peak) is higher with Lc = 0.5uH. This produces
  higher snubber discharge currents and hence higher
  transistor currents.
- Higher Vce values are observed during the current
  fall time period for Lc = 0.5uH.
The energy dissipated in the device in the various
stages of the cycle were calculated (in milli-Joules)
using the following formulae:

\[
E(\text{Tr}) = \frac{iT(pk)}{6} \cdot \frac{\text{Tr}}{6} \cdot (V_i + V_f) \quad \text{....(99)}
\]

\[
E(\text{Tds}) = iT(pk) \cdot V_d \cdot T_{ds} \quad \text{....(100)}
\]

\[
E(\text{To}) = V_{ce(sat)} \cdot iT(sat) \cdot T_o \quad \text{....(101)}
\]

\[
E(\text{Tf}) = V_{ce(Tf)} \cdot \frac{iT(Tf)}{6} \cdot T_f \quad \text{....(102)}
\]

\[
E(\text{Total}) = E(\text{Tr}) + E(\text{Tds}) + E(\text{To}) + E(\text{Tf})
\]

where \( E(\ ) \) = the energy dissipated in TR in the
appropriate part of the switching cycle
These results are shown graphically in Figure 7.5.
The losses in the transistor during the Df recovery
period are lower with Lc = 0.1 uH.
The losses during the dynamic saturation period are lower for \( L_c = 0.5 \text{ uH} \) - (voltage dropped across \( L_c \) rather than \( TR \)).

In the saturation period, the losses are comparable and dependent on \( V_{ce(sat)} \) only.

During the fall time period, higher losses occur with \( L_c = 0.5 \text{ uH} \) and this is due to the higher \( i_T \) and \( V_{ce} \) levels attained.

The total power loss in the devices are very similar (Figure 7.6) and this suggests that:

- the presence of \( L_c \) in the collector circuit does not reduce transistor losses
- higher circuit voltages are experienced with \( L_c \) in the circuit

The distribution of losses (% of total) in the transistors in the different periods of the switching cycle are ( @ 150A Iref):

<table>
<thead>
<tr>
<th>( L_c )</th>
<th>0.1uH</th>
<th>0.5uH</th>
</tr>
</thead>
<tbody>
<tr>
<td>%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

During,
- \( D_f \) recovery (\( T_r \)) | 35.4 | 38.1 |
- dynamic saturation (\( T_{ds} \)) | 5.3  | 2.4  |
- saturation (\( T_o \)) | 46.8 | 44.5 |
- fall time (\( T_f \)) | 12.5 | 15.0 |

The losses in the transistor occur mainly during the \( D_f \) recovery and the saturation period of the cycle.

Transistor losses can therefore be minimised by selecting fast recovery diodes (\( D_f \)) and a transistor with a low \( V_{ce(sat)} \). Other losses are less significant.
Transistor switching and power dissipation results for LC variation

Figure 7.4
Transistor power loss breakdown with and without collector circuit di/dt limiting inductance (Lc)

Total transistor losses for Lc = 0.5uH and Lc = 0.1uH

FIGURE 7.5

FIGURE 7.6
providing a turn-off snubber network is utilised. A nominal 0.1uH of inductance (Lc) could be used to aid current limiting under fault conditions.

7.3 Parallel Operation of Transistors

Measurement of the current in each of the transistors connected in parallel was not possible because the terminals of the devices were directly coupled. A guide to the mismatch in current sharing could however be ascertained from the device case temperature measurements. With reference to Figure 7.3, and allowing for a ± 5°C error in temperature measurement, the devices in each module, for Power Modules PM1 and PM2 are at approximately the same temperatures suggesting good current sharing.

Device No 2 in PM3 is at 82°C compared to 48°C and 54°C for the other two devices in the same stack. As the Vce(sat) are the same for all three devices, (base, collector and emitter terminals directly coupled), this could indicate that device No 2 is carrying a disproportionately high current relative to the others. A lesser mismatch in temperature is observed in PM4 where Device No 3 case temperature is 12°C higher than for the other two. The devices in PM5 were selected for a Vbe(sat) spread within 0.25V and showed similar case temperatures indicating that current sharing between the devices is adequate. This method of device selection for parallel operation is preferable as it incurs a minimal increase (< 5%) in cost compared to the alternative method of using

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additional passive components (emitter resistances and inductances). The resistances need to be at least 5 milliohms in value to be effective. The power dissipation in each resistor would then be approximately 50W/100A - a significant proportion of the total power module losses.

7.4 Power Source Performance

7.4.1 Comparisons with Power Sources using different power control technologies

The key specifications for the design of the power source is the accuracy, ripple content and frequency response. The results obtained are tabulated below and compared against other types of power sources:

<table>
<thead>
<tr>
<th>Type of machine</th>
<th>tR</th>
<th>tF</th>
<th>Ripple Amplitude (p/p)A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Series Linear Regulator</td>
<td>0.5</td>
<td>0.2</td>
<td>&lt; 3A</td>
</tr>
<tr>
<td>2. 15kHz Transistor chopper</td>
<td>1.0</td>
<td>1.5</td>
<td>&lt; 5A</td>
</tr>
<tr>
<td>3. 2.0kHz Transistor chopper</td>
<td>3.25</td>
<td>8.0</td>
<td>&gt; 40A</td>
</tr>
</tbody>
</table>

The use of a 15kHz modulation frequency (F0) has produced performance figures for the chopper set approaching that of the Series Linear Regulator power sources. In comparison, the low frequency Regulator power source has excessive current ripple and response times of 3.25ms at best.

Waveform comparisons are given in Figure 7.7.

7.4.2 Electrical Noise

The electrical conducted noise exceeds that specified
Comparison of current waveforms between power sources of different technologies

**SERIES LINEAR REGULATOR**

iL 100A/div  
T.B. 2.5ms/div

**15 kHz chopper SERIES SWITCHING REGULATOR**

iL 100A/div  
T.B. 2.5ms/div

**5 kHz chopper SERIES SWITCHING REGULATOR**

FIGURE 7.7
by FCC and VDE regulations. These regulations are not presently mandatory for arc welding equipment. As an example, the high frequency (1MHz), high voltages (15kV) used in TIG welding (for arc initiation) is an accepted part of the TIG welding process. It produces more severe electrical interference than that measured on this design of power source and has not been subjected to any regulatory controls to date. A typical filter circuit that could be used to reduce the conducted noise is shown in Figure 7.8a.

7.4.3 Acoustic Noise

In Section 6.3, the maximum noise measured under worst case operating conditions was 83.3 dbA. This is comparable to that produced by the SLR power source and 5 dbA (1.78 times) less than that produced by the low frequency chopper power sources.

7.4.4 Arc Instabilities

Three modes of arc instability were identified (Section 6.4) when welding with this design of power source. The presence of any form of instability in the arc process is unacceptable as it results in high levels of metal spatter, irregular weld bead shape, variable penetration and inconsistent droplet detachment. It was shown that the process instabilities could be prevented by restricting the arc current and voltages to those consistent with stable arc conditions. $\frac{di}{dt}$ limiting the falling edge of the pulsed current waveform also improved arc stability.
7.5 Operation of the Power Modules in parallel

The power module was shown to have an electrical limit of 250A and a thermal limit of 200A. Two power modules were connected in parallel to obtain the required 500A. Static current sharing between the modules was attained with the use of a balancing resistor connected between the output terminals of the two modules. A worst case mismatch of + 10A (Figure 5.38b) was achieved. Dynamic current sharing depends on the tolerance in Lc, Cs, Lf etc of each module, and is more difficult to control.

A more effective method of ensuring current sharing is shown in 7.8b. By using a current sensing element with a high bandwidth (e.g. Hall effect device) in each module output, static and dynamic sharing between the modules could be achieved by closed loop controlling the current in each power module.

7.6 Welding Performance

Pulsed Current MIG welding was successfully carried out in mild and stainless steel wires up to 1.6mm diameter. The susceptibility of this design of power source to arc instability has imposed restrictions on the process pulse parameters. Background currents (Ib) greater than 35A and minimum background voltage (Vb) values of 18 - 20V were found to be necessary for welding with high resistivity wires (ferrous materials). When welding with low resistivity wires (e.g. 99% pure Aluminium or its alloys), the arc voltage showed considerable variation (up to 5 - 10V) if the wire-
Filter networks required to reduce conducted EMI interference

FIGURE 7.8a

Independent closed loop control of the current in each power module to improve current sharing

FIGURE 7.8b
feeding was inconsistent due to drag in the torch lining or slippage in the wirefeeder-rolls. Under these conditions, the arc would grow uncontrollably in length and damage the torch contact tip. An arc voltage control (AVC) circuit was therefore used to regulate the arc length by controlling the wire feed rate. The response of this system (> 50 ms) is too long to be effective in situations where rapid arc length changes occur. It is therefore proposed that for dynamic arc length changes, the wire burn off rate should be used as the controllable loop parameter. A response of 1 - 2 ms to changes in arc length would then be possible.

Dip Transfer

Initial tests in the Dip Transfer mode have shown that a constant current characteristic power source produces weld properties at least as good as those using conventional constant voltage power sources. The main limitations of the Dip Process is high metal spatter and lack of fusion defects. These can be minimised by controlling Isc, Iarc and Td (Chapter 2). By limiting the short circuit currents to 450A, explosive metal detachment were eliminated. This in itself has reduced spatter levels. Further work needs to be carried out in investigating the effectiveness of the delay Td, in controlling spatter.

7.7 General

The original design of the power source has been extended to include three variants, two of which are shown in Figure (7.9).
Photographs of two variants of the 15kHz, chopper type of power sources

FIGURE 7.9

M450RS offers:
Pulsed CURRENT and Controlled Dip Transfer MIG Processes

M450 offers:
Synergic Pulsed Current MIG Transfer Process
8. CONCLUSIONS

8.1 A design of an advanced power source for MIG arc welding has been presented. The power conversion and control is based on a 15kHz transistor chopper type of regulator. The developed power source was shown to have characteristics and specifications superior to any other design of welding power source except for the series linear regulator based equipment.

8.2 The conversion of an unregulated 65V d.c. supply into a 450A controllable current for arc welding was achieved using two, 250A rated power modules.

8.3 The performance of the power modules were satisfactorily predicted from a computer model that was developed to include the effects of stray inductance, device characteristics and variable arc impedance.

8.4 A novel method of improving transistor switching performance at high currents (300A) has been developed. The transistors were dynamically de-saturated prior to applying a reverse bias. This was shown to reduce collector current storage and fall times.

8.5 Current regulation into a full load (40 milliohms) and shortcircuit (0.1 milliohms) loads was achieved using a combination of pulsewidth modulation and a variable modulating frequency. This control system produced current regulation of better than ± 5A over the full range of output currents up to 450A.

8.6 By operating the two power modules 180 degrees out of phase with each other, load ripple current amplitudes of less than 5A were achieved.
8.7 The output rise and fall times for pulsed conditions of \( \text{I}_{\text{ref}} \) were better than 1.5 ms.

8.8 Arc acoustic noise levels of less than 83.3 dbA were measured under worst case operating conditions. This is within existing legislation and 1.78 times (5 dBA) less than that of competitor products using 2kHz chopper controllers.

8.9 Three forms of arc instability, not previously reported, have been described.

8.10 The constant current characteristic has been used successfully for Pulsed Current Spray Transfer and Dip Transfer MIG welding using a range of welding wires and shielding gases.

8.11 A method of arc length control was found necessary due to the use of the constant current characteristic. The wire feed rate was adjusted automatically to maintain a given arc length under all operating conditions. This is a novel approach to the problem of arc length control which traditionally employs the variation of arc current to regulate against changes in arc length.

8.12 Suggested Future Work

The 15kHz chopper power source has been developed to a stage where the fundamental designs have been established. However, refinements and further development is necessary to improve reliability and enhance the present product specification:

a) The computer model needs to be modified to reflect changes in design that have resulted from the
practical work. These include the elimination of
collector circuit inductance (Lc), and the use of
lossless snubber circuits.

b) With the availability of higher current power
transistors, a single module rated at 500A could
be designed provided that the current sharing among
devices in parallel could be guaranteed. More
efficient methods of device cooling are also
necessary and these need to be investigated.

c) Mains and output filters need to be designed to
reduce the electrically conducted noise to within
FCC and VDE regulations.

d) The deregulation of the power source output current
associated with the welding of Aluminium needs to be
investigated further.

e) Current controlled Dip Transfer needs to be
developed further to prove that the improvements
in spatter reduction and fusion properties can be
repeated for a wider range of welding wires,
shielding gases and welding positions.

f) A more detailed investigation of the arc
instabilities reported in this work is needed.
These have stemmed directly as a result of
increasing the power bandwidth of the power source
- by increasing Fo and reducing the output inductance
(Lf). A relationship linking Fo, Lf and arc stability
limits needs to be developed. This will indicate the
maximum value of Fo that could be used in future
designs of switching power supplies for arc welding.
g) No attempt was made to analyse the closed loop stability criteria of the current control system for the whole range of arc impedances; this is a further area of research.

h) A thermal model needs to be developed that will compute device temperatures on a pulse by pulse basis ( @ 15kHz) and include the effects of transient thermal impedances of the devices and heatsinks.
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APPENDIX A

- Theoretical analysis of the transistor chopper
- Programme listings of the digital computer model of the transistor chopper
- Model open-loop operation data prints
- Model closed-loop operation data prints
THEORETICAL ANALYSIS OF THE TRANSISTOR CHOPPER CIRCUIT

Component Definition

\( V_I \) = input unregulated d.c. voltage source that is assumed to have zero source impedance and no ripple (infinite capacitance)

\( L_c \) = collector inductance for the purpose of \( \frac{di}{dt} \) limiting transistor current at turn on

\( T_R \) = Transistor switch operating at a high frequency (> 15kHz)

\( D_z \) = Zener diode for limiting the voltage across the transistor

\( R_z \) = effective series resistance of \( D_z \) and any added external resistance

\( D_s \) = snubber circuit charging diode

\( R_s \) = snubber circuit discharging resistor

\( L_s \) = snubber discharge current limiting inductance plus the self-inductance of \( R_s \)

\( C_s \) = snubber capacitance

\( L_{xs} \) = stray wiring inductance in snubber charging circuit

\( L_{xe} \) = stray wiring inductance in transistor emitter line

\( L_{xf} \) = stray wiring inductance in flywheel diode and negative supply line

\( D_f \) = Flywheel diode

\( L_f \) = Filter inductance

\( R_L \) = load resistance

\( V_L \) = load voltage (e.g. arc voltage)

\( R_{p}, \, C_p \) = resistor - capacitor network for \( \frac{dv}{dt} \) suppression across diodes \( D_f, \, D_c, \, D_s \).
Summary of Assumptions

a) That the supply has negligible series impedance and is ripple free

b) Diodes Dc, Ds have negligible recovered charge and constant forward voltage drop

c) Resistance of all inductor coils are negligible

d) Transistor saturation voltages are as per manufacturer's data

e) Diode Df forward voltage drop are as per manufacturer's data

f) Storage time in the transistor is negligible

g) All inductances are constant (i.e. assume air-cored inductors)

h) Load inductance included in Lf

j) Suppression networks Rp, Cp effective for a period < 1 uS and hence neglected in the analysis

Definition of Constants and Variables used in the Analysis - reference to Figure 1a,1b

In general, all upper case (Capitals) letters have been used to indicate initial and final values of variables and constants. Lower case letters are designated for time varying functions. Subscripts are used to clarify the variables. (As an exception, time varying voltages represented by upper case letter, U)

iL = current in inductor Lf and load

iT = transistor collector current

isl = snubber capacitor charging current

ist = snubber capacitor discharging current in transistor loop

isf = snubber capacitor discharge current in Df loop

isz = snubber capacitor current in Dz loop

iF = flywheel diode current

iL = current in Lf and load circuit

iz = current in Dz and Rz

ic = current in Lc
All voltages are measured with respect to the negative terminal of the supply $V_i$, unless stated differently.

$U_c$ = transistor collector voltage
$U_e$ = transistor emitter voltage
$U_{ce}$ = $U_c$ - $U_e$
$U_k$ = voltage at transistor end of $L_f$
$U_f$ = voltage at cathode of flywheel diode
$U_L$ = voltage across the load circuit
$U_s$ = voltage measured across snubber capacitor $C_s$
$U_p$ = voltage across $C_s$ and $L_{xs}$
$U_z$ = total voltage across $R_z$ and $D_z$
$U_t$ = transistor saturation voltage (varies with temperature, current, drive conditions etc)

$V_i$ = supply voltage at input of chopper circuit
$V_z$ = Zener diode breakdown voltage (assumed constant)
$V_L$ = Arc voltage

Other time related abbreviations used are:

$T_r$ = rise time of transistor emitter voltage relative to the collector voltage
$T_f$ = transistor current fail time (100% to 0% of $i_T$)
$T_{on}$ = transistor conduction in saturated mode
$T_{off}$ = transistor in blocking mode ($t_9$ minus $t_5$)
$t_{fr}$ = diode $D_f$ recovery from forward current conduction
$t_{rr}$ = diode $D_f$ recovery from reverse current conduction
$t_{rec}$ = $t_{fr}$ + $t_{rr}$ equals total reverse recovery time of $D_f$

Any other abbreviations used for variables quantities are defined local to the point of occurrence in the analysis.
A3.0 Description of circuit operation

It is assumed that the circuit has been operating for at least one cycle at the chopping frequency and current is established in the load. Flywheel diode \( D_f \) maintains the current flow in \( L_f \) and the load.

The start of the next cycle \((n)\), could occur in any one of periods VI to IX of the previous cycle \((n - 1)\) - Figure (i)- dependent on the pulsewidth. The currents and voltages at \( t_n = t_0 \) need to be evaluated. These form the initial conditions for Period I, of the new cycle \((n)\).

(i) if \( t_n = t_0 \) occurs in Period VI of the previous cycle \((t_5 < t_n-1 < t_6)\)

\( L_c \) will have been discharging its stored energy into snubber capacitor \( C_s \) as shown in Figure (ii)a. At \( t_n = t_0 \) the snubber charging current immediately transfers into \( D_z \) - Figure (ii)b in order to discharge \( L_{xs} \). \( C_s \) continues to charge until \( i_{sz} = 0 \). Only then does the discharge of \( C_s \) commence.

The current flowing in \( L_c \) at \( t_n < t_0 \) transfers immediately into \( T_R \) at \( t_n = t_0 \). The instantaneous values of the variables at \( t_n = t_0 \) become initial conditions for Period I and are subscripted as constants E.g. \( I_{c56} \) = current flowing in \( L_c \) at \( t_n = t_0 \)

(ii) if \( t_n = t_0 \) occurs in Period VII of the previous cycle \((t_6 < t_n-1 < t_7)\)

\( D_z \) has been conducting and providing a discharge path for \( L_c \). The energy stored in \( L_{xs} \) also discharges in a loop around \( D_z \) - Figure (ii)c. When \( T_R \) turns on, \( i_c \) is diverted into \( T_R \) immediately and \( i_{sz} \) continues to flow until \( L_{xs} \) is discharged - Figure (ii)d. Only then does the discharge of \( C_s \) commence.

The instantaneous values for these variables at \( t_n = t_0 \) become initial conditions for Period I of the next cycle and are subscripted as constant E.g. \( I_{c67} \).

(iii) if \( t_n = t_0 \) occurs in Period VIII of the previous cycle \((t_7 < t_n-1 < t_8)\)

\( L_c \) is discharging into \( D_z, R_z \) - Figure (ii)e. At \( t_n = t_0, i_c \) diverted immediately into \( T_R \). Zener diode \( D_z \) is reverse biased by \( T_R \) - Figure (ii)f.

The instantaneous values for these variables at \( t_n = t_0 \) become initial conditions for Period I of the next cycle and are subscripted as constants E.g. \( I_{c78} \).
(iv) If \( t_n = t_0 \) occurs in Period IX of the previous cycle (\( t_8 < t_{n-1} < t_9 \))

During Period IX, \( C_S \) has been in a resonant cycle of operation (charging, discharging) excited by \((V_s - V_i) - \text{Figure (ii} g,h\)).

The instantaneous values for these variables, at \( t_n = t_0 \) become initial conditions for Period I of the next cycle and are subscripted as constants E.g. \( I_{c89} \).

(v) In all of the above conditions, the transistor current can have an initial value which is not \( \frac{dI}{dt} \) limited. This occurs when \( I_c > 0 \) prior to transistor turn on.

For \( I_c < 0 \), the transistor current starts from zero and is \( \frac{dI}{dt} \) limited by \( L_c \).

(vi) It has been assumed that during all of the Periods VI to IX above, that the load current is continuous.

A3.1 Period I of the new cycle operates with \( t_0 < t_n < t_1 \)

Reference to Figure (iii)

Time reference \( t = t + t_0 \)

Description of circuit operation

At \( t_n = t_0 \), TR is turned on. The snubber capacitor \( C_S \) begins to discharge and Df current is commutated to TR.

(i) Analysis of snubber circuit discharge

The transistor turns on in a time \( T_r (\approx 250 \text{ ns}) \). The snubber circuit is forced to discharge into the transistor as shown in Figure (iii). Assuming that the discharge time of \( C_S > \) duration of Period I \( (t_1 - t_0) \), the discharge equation becomes,

\[
-(V_s - U_t) = (L_s + L_{xs}) \frac{d(I_{st})}{dt} + R_s I_{st} + \frac{1}{C_s} \int I_{st} \, dt
\]

Where \( V_s \) is one of \( V_{s56}, V_{s67}, V_{s78} \) or \( V_{s89} \)

From Appendix A4.4 and assuming

\[
\left[ \frac{R_s}{2} \right] < \frac{1}{(L_s + L_{xs}).C_s}
\]

\[
I_{st} = -(V_s - U_t).\sin[X_3.t].\exp(-R_s.t) \quad \ldots(103)
\]

\[
\frac{L_3.X_3}{L_{s+L_{xs}}} \quad \left( \frac{2.L_3}{L_{s+L_{xs}}} \right)
\]
where \( L_3 = L_s + L_{xs} \); \( X_3 = \sqrt{\frac{1}{L_3.C_s} - \frac{R_s^2}{2.L_3}} \)

Being a discharge current, the equation carries a negative sign.

(ii) Analysis of flywheel diode current \( (i_F) \)

During Period I, the load current is assumed to be constant such that,

\[ i_L = i_c + i_F \]

which when differentiated yields,

\[ - \frac{d(i_c)}{dt} = \frac{d(i_F)}{dt} \] \hspace{1cm} \ldots (104)

The equations describing Figure (iii) are:

\[ V_i - U_k - U_t = (L_c + L_{xe}).\frac{d(i_c)}{dt} \] \hspace{1cm} \ldots (105)

\[ U_k = - \frac{[(U_f + L_{xf}.d(i_F)]}{dt} \] \hspace{1cm} \ldots (106)

Substituting (104) (105) in (106) and rearranging and integrating w.r.t. time \( (t) \),

\[ i_F = I_{fo} + \frac{(U_t - V_i - U_f).t}{(L_{xf} + L_{xe} + L_c)} \] \hspace{1cm} \ldots (107)

with \( i_F = I_{fo} \) at \( t = t_0 \);

therefore \( i_c = i_L - i_F \) \hspace{1cm} \ldots (108)

Period I ends at \( t = t_1 \) with \( i_F = 0 \)

\[ t_1 = - \frac{I_{fo} (L_{xf} + L_{xe} + L_c)}{(U_t - V_i - U_f)} \] \hspace{1cm} \ldots (109)

(iii) General Equation for Period I

\[ i_c = i_c(t_0) + (i_L - i_F) \] \hspace{1cm} \ldots (110)

where \( i_c(t_0) \) is one of \( I_{c56}, I_{c67}, I_{c78}, I_{c89} \)

\[ i_T = i_c + ist; \text{ if } i_c(t_0) > 0 \] \hspace{1cm} \ldots (111)

\[ i_T = ist + (i_L - i_F); \text{ if } i_c(t_0) < 0 \] \hspace{1cm} \ldots (112)

\[ ist = -\frac{(V_s - U_t).\sin[X_3.t].\exp\left(-\frac{R_s.t}{L_3.X_3}\right)}{\frac{L_3.X_3}{(2.L_3)}} \] \hspace{1cm} \ldots (113)

if \( ist > 0 \), then set \( ist = 0 \)

\[ i_z = 0; \text{ isf} = 0; \text{ isz} = 0; \text{ isl} = 0; \] \hspace{1cm} \ldots (114)
\[ Up = Uz \]  
\[ = Ut \text{ (forced by transistor in saturation)} \]  
\[ Uce = Uce0 \left(1 - \frac{t}{Tr}\right); \text{ if } t > Tr, Uce = Ut \]  
where \( Uce0 = Uce \) at \( t=t0 \)  
\[ UL = VL + RL.iL \]  
\[ Uk = Uf + Lxf.\frac{d(iF)}{dt}; \text{ if } iF=0, Uk = Vi - Ut \]  
\[ Us = \int_{t0}^{t} dt = - \left[ Uf + Lxf.(Ut - Vi - Uf) \right] \frac{1}{(Lxf + Lxe + LC)} \]

From Appendix A4.6, this reduces to

\[ Us = -\left( Vs - Ut \right) \frac{X3 - \frac{1}{VL3.Cs} \exp\left(-\frac{Rs.t}{2.L3}\right) \sin\left(X3.t + X4\right)}{X3} + Vs \]

\[ -1 \]

Where \( X4 = \tan^{-1}\left(\frac{2.L3.X3}{Rs}\right) \)

\( Vs = \) one of \( Vs56, Vs67, Vs78, Vs89 \)

A3.2 Period II: \( tl < tn < t2; \) Flywheel diode \( Df \) recovery period

Reference to Figures (iii), (iv)

Time reference \( t = (t + tl) \)

Description of circuit operation

At time \( tn = tl \), \( Df \) forward current has been reduced to zero. Current continues to flow in the diode but in the reverse direction. This flow of current is due to minority carrier charge storage in the diode. The recovery current is made up of two parts - the forward and reverse recovery - Figure (iv)a. Period II analysis is for the forward recovery of the diode.

The load current is now supplied from \( Vi \) via the transistor, forcing \( iL \) to increase linearly.

The transistor continues to discharge the snubber capacitor. (This is assumed as being continuing as the discharge time has been arranged to be \( > (t2 - t0) \))

(1) Analysis of the forward recovery of diode \( Df \)

With reference to Figure (iv)b, the total recovered charge \( Qrr \) is given by
\[ Q_{rr} = \frac{1}{2} [t_{fr} + t_{rr}].I_{rm} \]

The equation assumes that \( d(i_F)/dt \) in the forward and reverse directions are linear functions of time.

Defining \( t_{rr} = S = \text{softness factor (<1)} \) \( \frac{t_{fr}}{t_{fr}} \)

From reference (40)

\[ t(fr) = \sqrt{\frac{3Q_{rr}}{(1 + S).d(iF)/dt}} \] ....(120)

(ii) Reverse diode current analysis

The reverse diode current is obtained from (107), giving

\[ I_{rm} = - \frac{(V_i + U_f - U_t).t_{fr}}{(L_xe + L_xf + L_c)} \] ....(121)

(iii) Snubber Discharge Analysis

The snubber discharge continues and the equations for 1st were derived previously and given by (103);

\[ \text{1st} = - \frac{(V_s - U_t).\sin[X3.t].\exp(-R_s.t)}{L3.X3} \frac{1}{2L3} \] ....(123)

(iv) Load current analysis

The flywheel diode current has been commutated to the transistor which now passes the load current.

From Figure (iv)b, the loop equation for \( i_L \) is,

\[ V_i-(L_xe+L_c).d(i_F)/dt-[d(i/L)/dt.(L_f+L_xe+L_c)]-i_L.R_L-V_L=0 \]

We also have \( (L_xe + L_c) \ll L_f \) (less than 1%). To keep the analysis simple, certain terms containing \( (L_xe + L_c) \) are assumed small and negligible compared to \( V_L \) and \( V_i \) giving

\[ V_i-(L_xe + L_c).d/dt(i_F + i_L)-L_f.d(iL)/dt -i_L.R_L-V_L = 0 \]

substituting for \( d(i_F)/dt \), derived from (107), we have

\[ V_i- (L_xe + L_c).(U_t - V_i - U_f)- L_f.d(iL) - i_L.R_L - V_L = 0 \]

Solving the differential equation for \( i_L \) (Appendix A4.4) gives
\[ i_L = \frac{(V_i - V_L) - (L_{xe} + L_c)(U_t - V_i - U_f)}{RL} [1 - \exp \left\{ RL(t - t_l) \right\}] + \frac{I_{fo}}{L_f} \exp \left\{ -RL(t - t_l) \right\} \quad \text{(124)} \]

Typical values are \( L_{xe} = 0.1 \ \mu\text{H}, \ L_c = 0.5 \ \mu\text{H}, \ V_i = 60\text{V}, \ U_f, \ U_t < 5\text{V} \)

Also, \( \frac{L_{xe} + L_c}{L_{xe} + L_{xf} + L_c} \approx 1, \ (U_t - U_f) \rightarrow 0 \)

Equation (124) could therefore be simplified to

\[ i_L = \frac{(2V_i - V_L)}{RL} + \frac{[I_{fo} - (2V_i - V_L)]}{L_f} \exp \left\{ -RL(t - t_l) \right\} \quad \text{(125)} \]

(v) General equation for Period II

\[ ic = i_L - i_F \quad \text{(126)} \]
\[ iT = ic + ist \quad \text{(127)} \]
\[ i_F = \frac{-(V_i + U_f - U_t)}{L_{xe} + L_{xf} + L_c} t + I_{fo} \quad \text{(128)} \]
\[ iz = 0; \ \text{isf} = 0; \ \text{isz} = 0; \ \text{isl} = 0; \quad \text{(129)} \]

\[ U_p = U_z = U_t; \ - \ \text{forced by transistor} \quad \text{in saturation} \quad \text{(130)} \]

\[ U_{ce} = U_t \quad \text{(131)} \]

\[ U_L = V_L + RL.i_L \quad \text{(132)} \]

\[ U_{k} = -(U_f + L_{xf}.(U_t - V_i - U_f)) \quad \text{(133)} \]

\[ U_s = -(V_s - U_t)[X_3 - \frac{1}{X_3}.\exp \{-R_s.t\}.\sin \left(\frac{X_3.t + X_4}{2L_3} + Vs\right) + \frac{X_3.C_s}{L_3} \quad \text{(134)} \]

Period II ends at \( t = t_2 \)

A3.3 Period III: \( t_2 < t_n < t_3 \): Recovery of \( D_f \) from reverse current flow

Reference Figure (iv) a, b

Time reference \( t = t + t_2 \)
Description of circuit operation

At \( t_n = t_2 \), most of the minority carrier charges in \( D_f \) were removed by the flow of reverse current. During this Period, this recovery current reduces to zero in time \( t_{rr} \).

Load current \( i_L \) continues to increase linearly;

\( C_s \) discharge is still incomplete and continues.

(i) Analysis of reverse recovery period of \( D_f \)

With reference to Figure (iv) b, for period \( t_{rr} \)

\[
\frac{d(I_F)}{dt} = \frac{I_{rm}}{S.t_{fr}} \text{ which when integrated yields,}
\]

\[
i_F = I_{rm} \left[ \frac{(t - t_2)}{S.t_{fr}} - 1 \right] ; \text{valid for } I_F < 0 \text{ only}
\] ....(135)

(ii) Snubber discharge analysis

The snubber discharge equation (103) is still applicable

\[
\begin{align*}
\text{ist} &= \left( V_s - U_t \right) \frac{\sin[X_3.t] \exp(-R_s.t)}{L_3.X_3} \exp\left( -\frac{R_3}{2.L_3} t \right)
\end{align*}
\] ....(136)

(iii) Load Current analysis

The load current is rewritten similarly from (125),

\[
\begin{align*}
i_L &= \left( 2V_i - V_L \right) + \left[ I_{fo} - \left( 2V_i - V_L \right) \right] \frac{\exp\left( -\frac{R_L}{L_f} \left[ t-t_1 \right] \right)}{R_L}
\end{align*}
\] ....(137)

Period III ends when \( I_F = 0 \).

(iv) General equation for Period III

\[
\begin{align*}
ic &= i_L - I_F \\
inT &= ic + ist \\
iF &= \frac{I_{rm} \left[ (t - t_2) - 1 \right]}{S.t_{fr}} \\
i_z &= 0; \ is_f = 0; \ isz = 0; \ isl = 0; \\
U_p &= U_z = U_t; \ - \text{forced by transistor in saturation}
\end{align*}
\] ....(138)....(139)....(140)....(141)....(142)....(143)

\[U_{ce} = U_t\] ....(143)
UL = VL + RL.iL ....(144)

\[ U_k = \frac{Lx_e \cdot I_{rm}}{S \cdot tfr} \] ....(145)

\[
U_s = (V_s - U_t) \left[ X_3 - \frac{1}{L_3 \cdot C_s} \cdot \exp\left[-\frac{R_s \cdot t}{2L_3}\right] \cdot \sin(X_3 \cdot t + X_4) \right] + V_s 
\] ....(146)

Period III ends when \( t = t_3 = t_2 + S \cdot tfr \) ....(147)

A3.4 Period IV: \( t_3 < t_n < t_4 \); Transistor Conduction Period

Reference Figures (v) a, b.

Time reference \( t = t + t_3 \)

Description of circuit operation

In this period, the load current continues to build up during the transistor "ON" time, the duration of which is determined by the current control system.

If the duration of Period III \( (t_3 - t_0) \) was < 5 \( \mu \)S, the snubber capacitor \( C_s \) would not have been fully discharged. \( C_s \) discharge therefore continues until \( V_s \) is zero. As the discharge circuit has been designed to be under-damped, a resonant cycle consisting of charging and discharging snubber circuit currents follows.

(1) Load Current analysis

In Figure (v)a, the load current is given by (125)

\[
i_L = \frac{(2V_i - V_L) + [I_{fo} - (2V_i - V_L)] \cdot \exp\left(-\frac{R_L \cdot (t - t_1)}{L_f}\right)}{R_L} + I_{fo} \cdot \exp\left(-\frac{R_L \cdot (t - t_1)}{L_f}\right) \] ....(148)

(11) Snubber circuit analysis

(a) In Figure (v)a \( V_s > 0 \) and its discharge continues giving

\[
\text{ist} = -\frac{(V_s - U_t) \cdot \sin(X_3 \cdot t) \cdot \exp\left[-R_s \cdot t\right]}{L_3 \cdot X_3} \cdot \frac{\sin(X_3 \cdot t + X_4) + V_s}{2L_3} 
\] ....(149)

This continues until \( \text{ist} = 0 \) (at \( t = t_a \)), after which the capacitor is negatively charged resonantly by ist to a voltage \( U_s(n) \).

(b) In Figure (v)b, the negative charge acquired by \( C_s \) is discharged into the load as shown. The discharge current is given by.
\[ isl = \frac{(V_i + Us(n) - UL) \cdot \sin(X_2(t-t_a)) \cdot \exp\left[-RL(t-t_a)\right]}{L_2 \cdot X_2} \]

where \((t - t_a) = t'\); time zero is at \(t_n = t_3\):

\[ X_2 = \sqrt{\frac{1}{\frac{L_2 \cdot C_S}{2L_2} + (RL)}} \]

\[ L_2 = (L_c + L_{xs} + L_{xe} + L_f) \]

When \(isl = 0\), (at \(t = t_b\)), \(Cs\) will be charged slightly positively to a voltage \(Us(n+1)\).

(c) the positive charge acquired by \(Cs\) will be discharged into the transistor as shown in Figure (v)a. The discharge current is given by,

\[ ist = -\frac{[Us(n+1) - Ut] \cdot \sin(X_3(t-t_b)) \cdot \exp\left[-Rs(t-t_b)\right]}{L_3 \cdot X_3} \]

where \(t - t_b = t''\)

This continues until \(ist = 0\); \(Cs\) is then charged negatively to \(Us(n + 2)\). When \(Us(n + k) < a\) specified voltage, this resonance can be terminated without affecting the accuracy of the model. The resonance discharge method was selected to give rapid discharge of \(Cs\) (< 5μS) - required for high frequency operation of the chopper.

(iii) General equation for Period IV

\[ ic = iL \]

\[ iT = ic + ist; \text{ if } ist < 0 \]

\[ iT = ic - isl; \text{ if } ist > 0 \]

\[ ist = -\frac{(Vs-Ut) \cdot \sin(X_3.t) \cdot \exp[-Rs.t]}{L_3 \cdot X_3} \]

( original discharge of \(Cs\) )

\[ ist = -\frac{[Us(n+1) - Ut] \cdot \sin(X_3.t'') \cdot \exp\left(-Rs.t''\right)}{L_3 \cdot X_3} \]

Resonant discharge/

\[ isl = \frac{(V_i+Us(n)-VL) \cdot \sin(X_2.t') \cdot \exp\left(-RL.t'\right)}{L_2 \cdot X_2} \]

of \(Cs\)

\[ iz = 0; isf = 0;isz = 0; iF = 0; d(iF)/dt = 0; \]

....(155)
\[ U_p = U_z = U_t \text{ forced by transistor in saturation} \]
\[ \ldots(156) \]
\[ U_{ce} = U_t \]
\[ \ldots(157) \]
\[ U_L = V_L + R_L i_L \]
\[ \ldots(158) \]
\[ U_k = U_L + L_f \cdot \frac{d(i_L)}{dt} \text{ giving,} \]
\[ U_k = U_L - \left[ \frac{I_f - (2V_i - V_L)}{R_L} \right] \cdot RL \cdot \exp\{-RL \cdot t\} \]
\[ \ldots(159) \]
The capacitor voltages are given by the resonant equations
\[ U_{sn} = \left( \frac{V_s - U_t}{X_3} \right) \left( \frac{1}{\sqrt{L_3 \cdot C_s}} \right) \cdot \exp\{-R_s \cdot t\} \cdot \sin\left[ X_3 \cdot t + \frac{X_4}{2\cdot L_3} \right] + V_s \]
\[ \ldots(160) \]
\[ U_{s(n+1)} = \left( \frac{V_s + V_i - V_L}{X_2} \right) \left( \frac{1}{\sqrt{L_2 \cdot C_s}} \right) \cdot \exp\{-R_L \cdot t'\} \cdot \sin\left[ X_2 \cdot t' + \frac{X_5}{2\cdot L_2} \right] + U_s(n) \]
\[ \ldots(161) \]
Where \[ X_5 = \tan^{-1}\left( \frac{2L_2}{X_2} \right) \]
\[ U_{s(n+2)} = \left( \frac{U_{s(n+1)} - U_t}{X_3} \right) \left( \frac{1}{\sqrt{L_3 \cdot C_s}} \right) \cdot \exp\{-R_s \cdot t''\} \cdot \sin\left[ X_3 \cdot t'' + \frac{X_4}{2\cdot L_3} \right] + U_{s(n+1)} \]
\[ \ldots(162) \]
(161), (162) repeat until \[ U_{s(n + k)} < 5V \] at which level the error has a negligible effect on the model.

Period IV ends at \[ t = t_4 = t_3 + t_{on} \]

A3.5 PERIOD V; \[ t_4 < t_n < t_5; \text{ Transistor turn off period} \]

Reference Figure (vi)

Time reference \[ t = t + t_4 \]

Description of circuit operation

At \[ t_n = t_4 \] the transistor receives a turn-off signal. Transistor current decreases to zero (storage time neglected).

The energy stored in inductances \( L_C, L_{xe} \) will force the snubber \( C_s \) to take over the transistor current during the fall time period (< 2.0 uS). The load current is unchanged over this short period and flywheel diode \( D_f \) remains reverse biased.
(i) Analysis of Transistor current
Assuming an exponential fall in transistor current

\[ i_T = I_{T4} \left(1 - \exp\left(-5 \frac{(t - t4)}{T_f}\right)\right) \]  

\[ \ldots (163) \]

(ii) Analysis of snubber circuit
The transistor current is transferred to the snubber and during this period, ic, il are assumed constant.
If Cs was charging resonantly at \( t_n = t4 \), then its value \( I_{L4} \) is added to the charging equation during this period.

If Cs was discharging, ist switches into a loop consisting of Ds, Rs and Ls and decays rapidly (250 nS)

Hence \( i_{sl} = i_T + I_{L4} \)  

\[ \ldots (164) \]

(iii) Voltage across the transistor
The transistor \( U_{ce} \) increases from its saturation level \( (U_t) \) to its blocking level \( (U_{ce}) \) and this is determined by the snubber circuit.
From Figure (vi),

\[ U_{ce} = L_{xs} \frac{d(i_{sl})}{dt} + \frac{1}{C_s} \int i_{sl} dt \]

which when evaluated gives

\[ U_{ce} = U_s(n) + L_{xs} I_{T4} \frac{5}{T_f} \exp \left[-5 \frac{(t-t4)}{T_f}\right] \]  

\[ \ldots (165) \]

\[ U_s = U_{s4+1} \frac{(t-t4).((I_{T4}+I_{L4})+T_f.I_{T4}.\exp[-5(t-t4)-1]}{C_s} \frac{5}{T_f} \]  

\[ \ldots (166) \]

Period V ends when \( i_T = 0 \)

(iv) General equation for Period V
\( i_l, i_c \) do not vary in this period and their values are given by (148), (152).

\( i_z = 0, i_{sf} = 0, i_{sz} = 0, i_{st} = 0, i_F = 0 \)  

\[ \ldots (167) \]

UL, Uk are unchanged during Period V and given by (158), (159).

Period V ends when \( t = t_5 = t4 + t_f \)
A3.6 Period VI; $t_5 < t_n < t_6$; Flywheel diode starts conducting load current

Reference Figure (vii).

Time reference $t = t + t_5$

Description of circuit operation

The transistor is in the blocking state and $C_S$ continues to charge, supplied from the energy stored in $L_c$ and stray inductances. As $i_C$ decreases, $i_F$ increases to maintain $i_L$. In the analysis, this is translated into 2 loop currents as shown in Figure (vii). $U_s$ continues to rise until $i_S = 0$. Period VI is terminated if $U_{ce}$ exceeds clamping zener voltage ($V_z$).

(i) Analysis of snubber current

$C_S$ has charged to a voltage $V_{s5}$ at $t_n = t_5$. $i_{sl}$ continues to flow and is derived from the $i_{sl}$ loop.

$$(V_i-U_k-V_{s5}) = (L_c+L_{xs}+L_{xe}+L_{xf}) \frac{d(i_{sl})}{dt} + \frac{i_{sl}}{C_s} \int i_{sl} \, dt$$

As $U_k \ll V_{s5}$, it can be neglected.

Differentiating, we have

$$0 = (L_c + L_{xs} + L_{xe} + L_{xf}) \frac{d^2(i_{sl})}{dt^2} + \frac{i_{sl}}{C_s}$$

and from Appendix A4.3, this has the general solution

$$i_{sl} = I_{L5} \cos \{w_0(t-t_5)\} \quad \ldots(168)$$

where

$$w_0 = \sqrt{\frac{1}{C_s(L_c + L_{xs} + L_{xe} + L_{xf})}}$$

(ii) Analysis of load current

The energy stored in $L_f$ is dissipated in the load by a flow of current in the $i_F$ loop. The loop equation for $i_L$ is

$$0 = U_f + \frac{d(i_L)}{dt}(L_{xf} + L_f) + R_Li_L + V_L$$

From Appendix A4.8, this reduces to

$$i_L = -(U_f+V_L) + [I_{L5}+(U_f+V_L)] \exp \left\{ -\frac{R_L(t-t_5)}{2(L_{xf} + L_f)} \right\} \quad \ldots(169)$$

(iii) Transistor blocking voltage analysis

$$U_{ce} = U_p = L_{xs} \frac{d(i_{sl})}{dt} + \frac{1}{C_s} \int i_{sl} \, dt$$
Substituting \(isl\) from (168) and solving,

\[
U_{ce} = V_{s5} + IL_5 \left( \frac{1 \pm \omega_0 L_{xs}}{C_s \omega_0} \right) \sin(\omega_0(t-t_5))
\]

...(170)

(iv) Snubber Capacitor Voltage Analysis

\[
U_s = V_{s5} + \frac{IL_5}{C_s \omega_0} \sin(\omega_0(t-t_5))
\]

...(171)

at \(t = t - t_5\), \(V_{sz} = V_{s5} + \frac{IL_5}{C_s \omega_0} \sin(\omega_0(t-t_5))\)

...(172)

(v) \(U_k = -[U_f + L_{xf} d(i_F)/dt]\)

\[
= U_f - \frac{[(U_f+V_L) + IL_5 \omega_0 \sin(\omega_0 t)] L_{xf}}{2(L_{xf}+L_f)}
\]

...(173)

The end of period VI occurs if \(U_{ce} > V_z\).

(vi) General equations for Period VI

\[
\text{ic} = isl = IL_5 \cos(\omega_0(t-t_5))
\]

...(168)

\[
\text{icz} = IL_5 \cos(\omega_0(t-t_5))
\]

...(174)

\[
i_F = (i_L - ic)
\]

...(175)

\[
i_z = 0; \text{it} = 0; \text{isz} = 0; \text{ist} = 0; \text{isf} = 0; \ldots(176)
\]

\[
U_L = V_L + RL_iL
\]

...(177)

A3.7 Period VII; \(t_6 < tn < t_7\)

Reference Figure (viii)a, b

Time reference \(t = t + t_6\)

Description of circuit operation

When \(D_z\) conducts, \(ic\) immediately flows into \(D_z, R_z\), clamping the transistor (\(U_{ce}\)) voltage to \(U_z\). The snubber stray inductance \(L_{xs}\) needs to discharge its stored energy resulting from the flow of \(isl\) in the previous period. It does so in a discharge loop (Figure viiib). Period VII ends when \(isz = 0\).

The load current continues to decay in the flywheel diode loop.

(i) Analysis of current \(ic\)

In the previous period, at \(tn = t-t_5\),
\[ ic = isl = Icz = IL5 \cdot \cos(\omega_0 [t-t5]) \]

Equation (174) gives the initial value for \( ic \) for \( tn > t6 \). The discharge of \( Lc \) now occurs in a different circuit – Figure (viii)a. The equation for this is,

\[ (Vi - Vz - Uk) = (Lc + Lxe + Lxf) \cdot \frac{d(ic)}{dt} + Rz \cdot ic \]

with \( ic = Icz \) as initial conditions.

\( Uk \ll Vz \) and hence neglected.

From Appendix A.7, this has a solution of the form,

\[ ic = \frac{(Vi-Vz) \cdot [1-\exp\left(-\frac{Rz(t-t6)}{Lc+Lxe+Lxf}\right)] + Icz \cdot \exp\left(-\frac{Rz(t-t6)}{Lc+Lxe+Lxf}\right)}{Rz \cdot (Lc+Lxe+Lxf)} \]

\[(178)\]

(ii) Snubber stray inductance discharge current analysis

At \( tn = t6 \), the current in snubber stray inductance, \( Lxs \), equals \( Icz \). This decay is shown in Figure (viii)b. Neglecting the forward voltage drops of \( Ds, Dz \),

\[ Lxs \cdot \frac{d}{dt} (isz) + \frac{1}{Cs} \int isz \, dt + Rz \cdot isz - Vsz = 0 \]

differentiating this yields,

\[ 2 \]

\[ Lxs \cdot \frac{d (isz)}{dt} + isz/Cs + Rz \cdot d(isz)/dt = 0 \]

The solution to this second order differential equation will depend on whether the roots are real, imaginary or equal. Solutions for each of these is given in Appendix A.4.4.

To test for the root conditions, the expression

\[ \frac{2}{2Lxs} \cdot \frac{1}{Lxs \cdot Cs} \]

is evaluated for typical values of \( Rz = 0.22R, Cs = 5 \, \mu F, Lxs = 0.1 \, \mu H \)

These give the two terms in the expression values of \( 4 \times 10^{-12} \) and \( 2 \times 10^{-10} \) respectively; these roots are assumed to be equal.

From Appendix A.4.4, the solution to the equation (with equal roots) is,
\( \text{isz} = \frac{[\text{Icz}-(t-t_6)(2Vz-Icz.Rz)]}{2Lxs} \cdot \exp\left[\frac{-Rz(t-t_6)}{(2Lxs)}\right] \quad \ldots(179) \)

(iii) The load \( iL \) continues to decay in the \( iL \) current loop. This is defined by equation (169)

\[
\begin{align*}
\text{iL} &= \frac{-(U_f + V_L) + \left[\text{IL5} + (U_f + V_L)\right] \exp\left(-\frac{R_L (t - t_5)}{2(L_xf + L_f)}\right)}{RL} \\
& \quad \ldots(180)
\end{align*}
\]

(iv) \( iF = (iL - ic) \) \ldots (181)

(v) \( iz = (ic - isz) \) \ldots (182)

Period VII ends when \( isz = 0 \).

(vi) \( Cs \) has charged to its peak value \( Vsz \) given by

\[
\begin{align*}
\text{Us} &= \frac{1}{Cs} \int \text{isz} \, dt\\
& = \frac{1}{Cs} \cdot \left[\frac{\text{Icz} - t(2Us(6) - Icz.Rz)}{2Lxs}\right] \exp\left(-\frac{Rz(t)}{(2Lxs)}\right) \\
\text{From Appendix A4.5, the solution is}
\end{align*}
\]

\[
\text{Us} = \frac{k_0}{k_1} \left\{k_3(t-t_6) + k_3/k_1 - k_2\right\} \exp\left(-k_1(t-t_6)\right) - \frac{k_3/k_1 - k_2}{2Lxs} \\
\] \ldots(183)

with \( k_0 = 1/Cs; \ k_2 = \text{Icz}; \ k_3 = \frac{(2Us(6) - Icz.Rz)}{2Lxs} \); \( k_1 = Rz/2Lxs \);

(vii) General equations for Period VII

\[
\begin{align*}
\text{isl} &= \text{ic} \quad \ldots(184) \\
iz &= (ic - isz) \quad \ldots(185) \\
iF &= iL - ic \quad \ldots(186) \\
iT &= 0; \ \text{isl} = 0; \ \text{ist} = 0; \ \text{isf} = 0; \quad \ldots(187) \\
\text{Uce} &= Vz + Rz.iz \quad \ldots(188) \\
UL &= VL + iL.RL \quad \ldots(189)
\end{align*}
\]

Period VII ends at \( t = t_7 = t_6 + tsz \) \ldots(190)

A3.8 Period VIII; \( t_7 < t_n < t_8 \)

Reference Figures (ix)

Time Reference \( t = t + t_7 \)
Description of Circuit operation

The energy in Lc and stray inductances are completely dissipated in Rz, Dz and the load during Period VIII. The load current continues to decay in the Df loop.

(i) Analysis of current ic

Reference Figure (ix)

\[ ic = \frac{Vi - Vz + (Icz - Vi - Vz) \cdot \exp\left(-\frac{Rz}{Rz} (t - t6)\right)}{Lx + Lxe + Lxf} \]

Also \( ic = iz \)

(ii) \( ic = 0 \) when

\[ tcz = \left[\frac{Lc + Lxe + Lxf}{Rz}\right] \ln \left[\frac{(Vz - Vi)/Rz}{Icz - (Vi - Vz)/Rz}\right] \]

(iii) \( iL = -(Uf + VL) + [IL5 + (Uf + VL)] \exp\left[-\frac{RL}{2} (t - t5)\right] \frac{1}{Lxf + Lf} \]

(iv) \( IF = (iL - ic) \)

(v) General equation for Period VIII

\[ ic = iz \]

\[ IF = iL - ic \]

\[ iT = 0; \; isl = 0; \; isf = 0; \; ist = 0; \;isz = 0; \ldots \]

\[ Uce = Vz + Rz.iz \]

\[ UL = VL + iL.RL \]

\[ Us = Vsz \]

Period VIII ends at \( t = t8 = t7 + tcz \)

A3.9 Period IX; \( t8 < tn < t9 \)

Reference Figure (x)a,b

Time reference \( t = t + t8 \)

Description of circuit operation

The load current continues to decay through Df.
At \( t_n = t_8 \), \( i_z \) was zero, causing \( D_z \) to go into its blocking state. This allows \( C_s \) to begin its discharge if \( V_{sz} > V_i \). In fact, a resonant cycle of current is set up by the difference voltage \( (V_{sz} - V_i) \).

(i) Load current analysis

The equation of the load current is obtained from (169).

\[
i_L = \frac{(U_f + V_L) + [IL5+(U_f+VL)\exp(-\frac{RL(t-t5)}{2(L_xf+L_f)})]}{RL}...
\]

(ii) Cs discharge cycle \((V_s > V_i)\)

Cs discharge loop is shown in Figure (x)a. The equation for \( i_{sf} \) is derived from the equation,

\[
(V_{sz}-V_i-U_f) = \frac{1}{C_s} \int i_{sf} \, dt + (L_{xe}+L_{xs}+L_{xf}+L_{c}+L_s) \frac{d(isf)}{dt} + R_s.isf
\]

This is the second order differential equation with solution dependent on the nature of the roots of the equation.

\[
2
\frac{1}{L_k.C_s} > (R_s^2) \text{ (imaginary roots)}
\]

The term \( \left(\frac{R_s}{2L_k}\right) \) needs to be evaluated for

\[
R_s = 0.3R; \quad C_s = 5.0 \, \mu F; \quad L_k = L_{xe}+L_{xf}+L_{xs}+L_{s} = 3 \, \mu H
\]

This gives \( \frac{1}{L_k.C_s} > \left(\frac{R_s}{2L_k}\right) \) (imaginary roots)

From Appendix A4.4, with \( i_{sf} = 0 \) initially,

\[
i_{sf} = -\frac{[Us(2p-1)-V_i-V_f].\sin(X_k(t-t8)).\exp(-Rst(t-t8))}{L_k.X_k}...
\]

Where \( X_k = \sqrt{\frac{1}{L_k.C_s} - (\frac{R_s}{2L_k})^2} \)

\( U_s (1) = V_{sz} \)

\( p = 1, 2, 3 \ldots \ldots n = \text{resonant cycle number.} \)

The discharge ends when \( i_{sf} = 0 \), and occurs at

\[
t = p.\frac{II}{X_k}...
\]

(ii)b Capacitor voltage \( U_s \) is given by

\[
U_s = \frac{1}{C_s} \int i_{sf} \, dt \text{ which from (203) and Appendix A4.6 yields}
\]
Us(2p) = \frac{Us (2p-1) \cdot (Xk - A0)}{Xk} \cdot \frac{1}{LK} \cdot \frac{\sin[Xk(t-t8)+X0]}{Cs} + Vsz

where X0 = \tan \left(\frac{2Lk \cdot Xk}{Rs}\right)

A0 = \exp \left(-\frac{Rs \cdot t}{2Lk}\right)

(iii) a Cs Charging cycle

The capacitor will be discharged to less than Vi due to the underdamped resonant current. This starts (at t = ts0) a charging cycle for Cs and is shown in Figure (x)b. This is an undamped circuit if the diode voltage drops are neglected. \(isl\) is the discharging current and derived from

\[(Vi + Us(2p) - Uk) = (Lc + Lxs + Lxe + Lxf) \cdot \frac{\mathrm{d}(isl)}{\mathrm{d}t} + \frac{1}{Cs} \int isl \, dt\]

where \(Uk \ll Vi\). From Appendix A4.4 (with \(R = 0, I_0 = 0\)) in equations (231),

\[isl = \left(\frac{Vi + Us (2p)}{Ly \cdot wm}\right) \cdot \frac{\sin[wm(t - ts0)]}{Ly \cdot wm}\]

where \(Ly = Lc + Lxs + Lxe + Lxf\)

\[wm = \sqrt{\frac{1}{Ly \cdot Cs}}\]

\[isl = 0 \text{ when } t = \frac{p.II}{wm}\]

(iii)b capacitor voltage \(Us\) is given by,

\[Us (2p + 1) = \frac{1}{Cs} \int isl \, dt\]

\[Us (2p + 1) = \left[\frac{Vi - U(2p)}{Ly \cdot wmCs}\right] \cdot \left[1 - \cos\{wm(t-ts0)\}\right] + Us(2p)\]

Equations for charge and discharge cycles are repeated until the value of \(Us\) falls below 5V when this resonance is presumed negligible.

Period IX ends at \(t = t9 = t8 + ton\) - the end of the cycle

(iv) General equations for Period IX

If capacitor Cs is charging

\[ic = isl = \left[\frac{Vi - Us (2p)}{wm \cdot Ly}\right] \cdot \sin[wm(t-ts0)]\]

If capacitor Cs is discharging
ic = isf = \(-[Us(2p\!+\!1)\!-\!Vi\!-\!Uf] \frac{\sin(Xk.t)}{2Lk} \exp\{-Rs(t-t8)\}\)

\(iF = iL - ic\) 

\(iT = 0; iz = 0; ist = 0; isz = 0;\)

\(\text{Uce} \quad \text{Us as voltage drop across Lxs is small}\)

\(UL = VL + iLRL\) 

\(t9 = t8 + ton\)

---

**A.4 Generalised solutions to equations used in the analysis**

Abbreviation: L.T. = Laplace Transform

I.L.T. = Inverse Laplace Transform

Reference to Figures (xi) - (xiv)

**First order differential equation with constant coefficients**

**A.4.1 R-L series network with initial conditions \(i=Io\)**

\(V = L(di/dt + R.i) \quad \text{with} \quad i = Io \quad \text{at} \quad t = 0\)

L.T. of (215) gives

\(V/s = L.\left[s.i(s) - Io\right] + R.i(s)\)

which reduces to:

\(i(s) = V-L.Io/s(sL+R)\)

I.L.T. of (216) gives

\(i(t) = V/R + (Io - V/R) . \exp(-R.t)/L\)

**A.4.2 R-C series network with initial conditions \(U=Vo\)**

(a) \(V = Ri + 1/C \int i \, dt \quad \text{with} \quad i = 0 \quad \text{at} \quad t = 0\)

L.T. of (218) gives \(V/s = R.i(s) + i(s)/sC\)

which reduces to

\(i(s) = \frac{V}{R} . \frac{1}{s+1/CR}\)

I.L.T. of (219) gives

\(i(t) = \frac{V}{R} . \exp(-t/CR)\)

(b) capacitor voltage \(U = 1/C \int i(t) \, dt; U=Vo \quad \text{at} \quad t=0\)

\(= 1/C \int V/R \exp(-t/CR) \, dt\)

which yields

\(U = Vo + V(1 - \exp(-t/CR))\)
A4.3 L-C series network with initial conditions

Loop current is given by the differential equation

\[(V - V_0) = L \frac{di}{dt} + \frac{1}{C} \int idt \]  \(\ldots(221)\)

As no damping terms occur, the general solution is

\[i(t) = A \sin(\omega t) + B \cos(\omega t) \]  \(\ldots(222)\)

\[\frac{di}{dt} = A \omega \cos(\omega t) - B \omega \sin(\omega t) \]  \(\ldots(223)\)

at \(t = 0, i = I_0, V = V_0\)

from equation (222),

\[I_0 = B\]

from equation (223)

\[\frac{(V - V_0)}{L} = A \omega\]

Substituting for \(A, B\) in (222) yields

\[i(t) = \frac{(V - V_0)}{\omega L} \sin(\omega t) + I_0 \cos(\omega t) \ldots(224)\]

Second order differential equations with constant coefficients

A4.4 R-L-C. series network with initial conditions \(i = I_0; U = V_0\)

\[(V - V_0) = L \frac{di}{dt} + R i + \frac{1}{C} \int idt \]  \(\ldots(225)\)

which when differentiated yields,

\[0 = \frac{d^2 i}{dt^2} + R \frac{di}{dt} + \frac{i}{C} \]  \(\ldots(226)\)

Using D operators (226) becomes;

\[0 = L D^2 + R D + \frac{i}{C} \quad \text{with} \quad D = \frac{di}{dt} \]

with roots \(s_1 = -\frac{R}{2L} + \frac{1}{LC} \ldots(227)\)

\[s_2 = -\frac{R}{2L} - \frac{1}{LC} \ldots(228)\]

The general solution for \(i(t) = A \exp(s_1 t) + B \exp(s_2 t)\)

at \(t = 0, i = I_0\) giving \(I_0 = A + B\)

at \(t = 0 \frac{di}{dt} = \frac{(V - V_0)}{L},\) giving

\[\frac{(V - V_0)}{L} = A s_1 + B s_2\]
Solving for $A$, $B$ and substituting

$$i(t) = \frac{[L \cdot I_0 \cdot s_1 - (V - V_0)] \exp(s_2 \cdot t) + [(V - V_0) - L \cdot I_0 \cdot s_2] \exp(s_1 \cdot t)}{L \cdot (s_1 - s_2)}$$

...(229)

which is the general solution to the equation.

The precise solution will depend on the nature of $s_1$, $s_2$ and in particular the value of the term

$$2 \frac{(R/2L) - 1/L.C}{2}$$

A4.4a if $(R/2L) > 1/L.C$, $i(t) = \text{equation (229)}$

A4.4b if $(R/2L) = 1/L.C$ $s_1 = s_2$

In equation (229), $i(t) = 0$ if direct substitution of $s_1$, $s_2$ used

Invoking L'Hopital's rule which states that if

$$f(x) = \frac{g(x)}{h(x)}$$

such that with $x \to k$, $g(k) \to 0$, $h(k) \to 0$,

$$f(k) = \frac{g'(x)}{h'(x)}$$

where prime denotes differentiation $f'(x)$ with respect to $x$.

This applies to equation for $i(t)$ and selection $s_2$ as the variable for $x$, L'Hopital's rule reduces equation (229) to,

$$i(t) = \frac{L \cdot I_0 \exp(s_1 \cdot t) + t \cdot [L \cdot I_0 \cdot s_1 - (V - V_0)] \exp(s_2 \cdot t)}{L}$$

as $s_1 = s_2 = -R/2L$

$$i(t) = \frac{[I_0(-L + R \cdot L \cdot t) + t \cdot (V - V_0)] \exp(-R \cdot t)}{L \cdot 2L}$$

$$= \frac{[I_0(1 + R \cdot t) + (V - V_0) \cdot t] \exp(-R \cdot t)}{L \cdot 2L}$$

... (230)

A4.4c if $(R/2L) < 1/L.C$ $s_1, s_2 = -R/2L + j \frac{1}{1/L.C - (R/2L)}$

$$i(t) = \frac{\exp(-R \cdot t/2L)}{L(2jB)} \left[[L \cdot I_0(-R/2L + jB) - (V - V_0)] \exp(-jB \cdot t) + \right.$$

$$\left.((V - V_0) - L \cdot I_0(-R/2L - jB)) \exp(jB \cdot t)\right]$$

which when simplified gives

$$i(t) = \exp(-R \cdot t/2L) \cdot \frac{\sin(B \cdot t)((V - V_0) + I_0.R/2) + B.L.I_0 \cos(B \cdot t))}{BL}$$

...(231)

Where $B = \sqrt{\frac{1}{1/L.C - (R/2L)}}$
A4.5 Integral of the form

\[
f(t) = k_0 \int (k_2 - t.k_3). \exp(-k_1.t) \, dt \quad \ldots \ldots (232)
\]

\[
= \int k_0.k_2 \exp(-k_1.t) \, dt - \int k_0.k_3.t \exp(-k_1.t) \, dt
\]

\[
= \int A \, dt - \int B \, dt
\]

\[
\int A \, dt = \left[ -\frac{k_0.k_2}{k_1} \exp(-k_1.t) + C_1 \right]
\]

\[
\int B \, dt = \frac{k_0.k_3}{k_1} \left[ -t \exp(-k_1.t) \right] - \int \left[ -\frac{1}{k_1} \exp(-k_1.t) \right] \, dt
\]

\[
= k_0.k_3 \left\{ \left[ -\frac{1}{k_1} \exp(-k_1.t) + C_2 \right] \right\} - \frac{2}{k_1} \left[ -\frac{1}{k_1} \exp(-k_1.t) + C_3 \right]
\]

Rearranging,

\[
f(t) = k_0/k_1 \left[ k_3(t+1/k_1)-k_2 \right] \exp(-k_1.t) + f(o) - k_0/k_1 \left[ (k_3/k_1-k_2)/k_1 \right] \quad \ldots \ldots (233)
\]

Substitute for constants \( k_0 - k_4 \) from relevant equations.

If at \( t = 0 \), \( f(t) = f(o) \) where

\[
f(o) = \frac{k_0}{k_1} (k_3/k_1 - k_2) + k_4
\]

Therefore \( k_4 = f(o) - \frac{k_0}{k_1} (k_3 - k_2.k_1) \)

\[
f(t) = \frac{k_0}{k_1} \left[ \left( k_3.t+k_3/k_1-k_2 \right) \exp(-k_1.t) \right] - \frac{k_0}{k_1} \left[ (k_3/k_1-k_2)/k_1 \right] + f(o)
\]

A4.6 Integral of the form

\[
U(t) = \frac{1}{C} \int I. \exp(-p.t). \sin[m.t] \, dt \quad \ldots \ldots (234)
\]

rewrite \( \sin[m.t] = \left[ \exp(jm.t) - \exp(-jm.t) \right]/2j \) and simplify equation,

\[
U(t) = I/2JC \int \left( \exp(-(p-jm)t) - \exp(-(p+jm)t) \right) \, dt
\]

\[
= I/2JC \left\{ \exp(-(p+jm)t) - \exp(-(p-jm)t) \right\} \left[ \frac{1}{(p+jm)} - \frac{1}{(p-jm)} \right] + C
\]

if at \( t = 0 \), \( U(t) = V_0 \)

\[
U(t) = I/2JC \left\{ \left[ (p-jm) \exp(-(p+jm)t) - (p+jm) \exp(-(p-jm)t) \right] + V_0 + \frac{2}{2} \right\}
\]

\[
+ I.m/C(p + m )
\]
\[ U(t) = -I \exp(-pt) \left\{ \frac{p[\exp(-jmt) - \exp(jmt)] - jm[\exp(-jmt) + \exp(jmt)]}{2jC(p + m)} \right\} + Vo + \frac{Im}{C(p + m)} \]

with \( \cos[m.t] = \frac{\exp(jmt) + \exp(-jmt)}{2} \)
\( \sin[m.t] = \frac{\exp(jmt) - \exp(-jmt)}{2j} \)
\[ U(t) = I \exp(-pt) \left\{ \frac{-p.2j \sin(mt) - m.2j \cos(mt)}{2jC(p + m)} \right\} + Vo + \frac{Im}{C(p + m)} \]

Finally \[ U(t) = -I \exp(-pt) \left\{ \frac{[p.\sin(mt) + m.\cos(mt)]}{2} + Vo + \frac{Im}{C(p + m)} \right\} \]

In the analysis, \( p = \frac{R}{2L}; m = \frac{1}{L.C} - \frac{R}{2L} \);
\[ I = -\frac{V}{2L.X} \]

Substituting these in (235) yields
\[ \frac{p}{(p + m)} = \cos(k); \frac{m}{(p + m)} = \sin(k) \]
\[ k = \tan \left( \frac{m}{p} \right) \]
Equation (235) becomes
\[ U(t) = Vo + \left( \frac{I.m - I.\exp(-pt).[\sin(mt+k)]}{2jC(p + m)} \right) \]

Substituting for \( p, m, I, k \)
\[ U(t) = Vo + \frac{V}{2X} \left[ X - \sqrt{1/L.C} \exp - \frac{R.t}{2L} \sin(Xt + k) \right] \]

\textit{A4.7 Solve Laplace equation of the form}

\[ V/s = L[s.i(s) - Io] + R.i(s) \]

collecting for \( i(s) \), we have
\[ I(s) = \frac{(V/s + L.Io)/(sL + R)} \]
rеrраrrаgіng \( i(s) \) yіelds
\[ i(s) = \frac{V/[s.L(s + R/L)] + Io/(s + R/L)} \]

\textit{І.І.Т gіvеs:}
\[ i(t) = \frac{V/R (1 - \exp[-R.t/L]) + Io \exp [-R.t/L]} \]

\text{(237)}
Typical circuit and device current waveforms for one cycle of operation of the chopper.

FIGURE ia
Chopper power circuit inclusive of stray impedances and protection circuitry

FIGURE 1b

Chopper circuit adapted for computer modelling

FIGURE 1c
Conditions as the circuit commutates from cycle \((n-1)\) to cycle \((n)\)
Circuit conditions during Period I

Figure (iv)a

Details of Df reverse recovery

Figure (iv)b

Circuit conditions for Periods II & III

Figure (v)a

snubber discharging

Figure (v)b

Circuit conditions for period IV

Figure (v)
Circuit conditions for Period VII

Figure (viii)a

Dz in partial conduction

Figure (viii)b

Dz in full conduction

transfer of iC from snubber circuit to Dz

Circuit conditions for Period VIII

Figure ix

Circuit conditions for Period IX
(snubber discharging)

Figure (x)a

Circuit conditions for Period IX
(snubber charging)

Figure (x)b
**Figure xi**
R – L network

**Figure xii**
R – C network

**Figure xiii**
L – C network

**Figure xiv**
R – L – C network
DEFINITION OF MAIN PROGRAM VARIABLES, CONSTANTS ETC

BILREF = BACKGROUND CURRENT REFERENCE (PULSE ONLY)
CS = SNUBBER CAPACITANCE
CILREF = CONTINUOUS CURRENT REFERENCE
DJC = F/Diode JUNCT-CASE THERMAL RESISTANCE
EFF = EFFICIENCY OF MACHINE
ERROR = CURRENT ERROR CONVERTED TO CONTROL VOLTAGE (50A=1V)
ERRA = CURRENT ERROR (AMPS)
F = CHOPPING FREQUENCY
FO = ACTUAL CHOPPING FREQUENCY
G = CURRENT CONTROL LOOP GAIN
HILREF= PEAK CURRENT REFERENCE (PULSE ONLY)
IC = COLLECTOR CIRCUIT CURRENT
IF = F/Diode CURRENT
IL = LOAD CURRENT
IS, ISF, ISL, IST, ISP, ISR, ISK, IZS = VARIOUS COMPONENTS OF SNUBBER CHARGING AND DISCHARGING CURRENTS
IT = TRANSISTOR CURRENT
IZ = ZENER DIODE CURRENT
ISM = PEAK SNUBBER CURRENT
ITM = PEAK TRANSISTOR CURRENT
IFM = PEAK F/Diode CURRENT
JL = PULSE PEAK-BACKGROUND CYCLE COUNTER
J = BACKGROUND-PEAK PULSE CYCLE COUNTER
K = CYCLE NUMBER
LC = COLLECTOR INDUCTANCE
LF = OUTPUT INDUCTANCE
LS = SNUBBER DISCHARGE CIRCUIT INDUCTANCE
LXE = EMITTER CIRCUIT STRAY INDUCTANCE
LXF = F/Diode CIRCUIT STRAY INDUCTANCE
LXS = SNUBBER CAPACITOR INDUCTANCE
LPW = PULSE WIDTH (MICROSECONDS)
LPWM = PULSE WIDTH (NANOSECONDS)
NTRAN = NUMBER OF POWER TRANSISTORS IN PARALLEL
OPI = OUTPUT LOAD CURRENT
OPV = OUTPUT LOAD VOLTAGE
PT = INSTANTANEOUS TRANSISTOR DISSIPATION
PS = INSTANTANEOUS SNUBBER CIRCUIT DISSIPATION
PL = INSTANTANEOUS LOAD POWER
PRFD = F/Diode RECOVERY POWER LOSS (INSTANTANOUS)
PLLOSS = TOTAL POWER MODULE + OTHER MACHINE LOSSES
PDIODE = TOTAL F/Diode LOSSES
PSNUB = TOTAL SNUBBER CIRCUIT LOSSES
PTRAN = TOTAL TRANSISTOR LOSSES
PLOAD = TOTAL LOAD POWER
PTOT = TOTAL INPUT POWER (KW)
QR = MINIMUM F/Diode RECOVERED CHARGE
RZ = ZENER CIRCUIT RESISTANCE
RS = SNUBBER DISCHARGE RESISTANCE
RL = LOAD CIRCUIT RESISTANCE
RIPPLE = LOAD RIPPLE CURRENT AMPLITUDE (PEAK-PEAK)
RCH = TRANSISTOR CASE-H/SINK THERMAL RESISTANCE
RHA = TRANSISTOR H/SINK-AMBIENT THERMAL RESISTANCE
RCHD = F/Diode CASE-H/SINK THERMAL RESISTANCE
RHAD = F/Diode H/SINK-AMBIENT THERMAL RESISTANCE
S = F/Diode RECOVERY FACTOR
TF = TRANSISTOR CURRENT FALL TIME
TR = TRANSISTOR TURN ON TIME
TRJC = TRANSISTOR JUNCT-CASE THERMAL RESISTANCE
* PRESET/INITIAL CONDITIONS FOR SIMULATION PROGRAM
*
*
001.0  ! =S  ;F/Diode recovery factor
000.22 ! =RZ  ;Zener resistance
000.10 ! =RS  ;Snubber discharge resistance
000.40 ! =RL  ;Load resistance
001.50 ! =UD  ;Diode forward volt drop
060.00 ! =VI  ;D.C. supply voltage
015.00 ! =VL  ;Load standing voltage
001.50 ! =UTR ;Transistor saturation voltage
130.00 ! =VZ  ;Zener diode voltage
00.60E-06 ! =LC  ;Collector inductance
60.00E-06 ! =LF  ;Output inductance
01.50E-06 ! =LS  ;Snubber discharge inductance
00.20E-06 ! =LXE ;Emitter stray inductance
00.20E-06 ! =LXF ;F/Diode path stray inductance
00.20E-06 ! =LXS ;Snubber capacitor stray inductance
04.00E-06 ! =CS  ;Snubber capacitance
1.500E-06 ! =TF  ;Transistor current fall time
00.25E-06 ! =TR  ;Transistor turn on time
10.00E-06 ! =QR  ;F/Diode recovered charge
00.00 ! =IC(1) ;Initial value of IC
00.00 ! =IF(1) ;Initial value of IF
00.00 ! =IL(1) ;Initial value of IL
 0.0   ! =IS(1) ;Initial value of IS
 0.0   ! =IT(1) ;Initial value of IT
 0.0   ! =IZ(1) ;Initial value of IZ
60.00 ! =UCE(1) ;Initial value of UCE
60.00 ! =US(1) ;Initial value of US
 15.00 ! =UL(1) ;Initial value of UL
15.00E+03 ! =FREQUENCY (F)
0250.0  ! =CILREF ;Peak current reference
100.0  ! =LOOP_GAIN
000.10 ! =TRANSISTOR JUNCTION-CASE THERMAL RESISTANCE
000.10 ! =TRANSISTOR CASE-HEATSPRING THERMAL RESISTANCE
000.05 ! =DIODE JUNCTION-CASE THERMAL RESISTANCE
000.07 ! =TRANSISTOR HEATSPRING-AMBIENT THERMAL RESISTANCE
000.05 ! =DIODE CASE-HEATSPRING THERMAL RESISTANCE
000.07 ! =DIODE HEATSPRING-AMBIENT THERMAL RESISTANCE
025.00  ! =AMBIENT TEMPERATURE
003   ! =NTRAN
0050.0  ! =BACKGROUND CURRENT
END
*
*
*****
THE PROGRAM HAS BEEN RUN ON THE GEC 4190 SERIES COMPUTER
BETWEEN 1.04.63 AND 31.07.64 AND ALSO ON A VAX 11/78 SYSTEM
AT THE OPEN UNIVERSITY BETWEEN 1.09.81 AND 31.03.83.

THIS PROGRAM LISTING IS THAT OF A DIGITAL COMPUTER SIMULATION
OF A 15 KHz 250 AMPERE TRANSISTOR CHOPPER OPERATING OFF AN
ELECTRICALLY ISOLATED 65 VOLTS D.C. SUPPLY.

A COMBINATION OF THESE MODULES IS USED TO PRODUCE A
WELDING POWER SOURCES FOR METAL INERT GAS (MIG) AND
TUNGSTEN INERT GAS (TIG) WELDING PROCESSES.

THE LOAD PRESENTED TO THE MODULES CAN VARY FROM AN
OPEN CIRCUIT TO NEAR SHORT CIRCUIT (<< .002 OHM RESISTANCE)
AND VICE VERSA IN A TIME PERIOD OF TYPICALLY 100 micro SECONDS.
The program is split into 10 segments derived from an analysis
of the transistor current amplitude variation over one cycle
of operation.
Two further segments are included to cover data file management
and the control of the chopper frequency and pulse width under
closed loop control of the load current.

SEGMENT (a) - OPEN DATA FILES
- OPEN DATA FILES FOR INITIAL CONDITIONS
- READ INITIAL CONDITIONS FROM DATA FILES
- EVALUATE REGULARLY OCCURING FUNCTIONS

DEFINE VARIABLES/DIMENSION, DATA TYPE ETC
DIMENSION IC(9999), IF(9999), IL(9999), IS(9999), IT(9999), IZ(9999),
UCE(9999), UU(9999), US(9999), IZS(9999), ISM(9999), PT(9999),
PS(9999), PF(9999), PL(9999)
DIMENSION ISF(9999), ISL(9999), IST(9999), ISZ(9999), ISP(9999)
REAL LC, LF, LS, LXE, LXF, LXS, L2, L3, IC, IF, IL, IS, IT, IZ, ISF, ISL,
IST, ISZ, IY, ICZ, ISP, ICL, L1, IZS, ISM, ISN, LG, ierr, ITM, IFM

OPEN DATA FILES

CALL CONECT('.DATA/NEW',6)
CALL CONECT('.PSET/OLD',4)
CALL CONECT('.CLDAT/NEW/L',5)
NuRite=0

READ INITIAL CONDITIONS FROM DATA FILE '.PSET'

READ(4,1000)S,RZ,RS,RL,UD,VI,VL,UTR,VZ,LC,LF,LS,LXE,LXF,LXS,C5,
-T,TR,QR,IC(1),IF(1),IL(1),IS(1),IT(1),IZ(1),UCE(1),US(1),
-UL(1),F,HILREF,G,TRJC,RCH,DCJ,RHA,RCHD,RHAD,TA,NTTRAN,BILREF
1000 FORMAT(9(1X,F6.2/),10(1X,E9.2/),9(1X,F6.2/),E9.2/,2(F6.2/),
EVALUATION OF REGULARLY OCCURRING FUNCTIONS

\[ L_1 = L_C + L_XE + L_XF \]
\[ L_2 = (L_C + L_XE) - (L_LX) \]
\[ L_3 = (L_SE + L_XS) \]
\[ L_K = (L_XE + L_XF + L_XS + L_SE + L_C) \]
\[ L_Y = (L_C + L_XS + L_XE + L_XF) \]
\[ X_2 = \sqrt{\frac{1}{(L_2 \cdot C_S) - (R_L / (2 \cdot L_2))^2}} \]
\[ X_3 = \sqrt{\frac{1}{(L_3 \cdot C_S) - (R_S / (2 \cdot L_3))^2}} \]
\[ X_4 = \arctan\left(\frac{2 \cdot L_3 \cdot X_3}{R_S}\right) \]
\[ X_5 = \arctan\left(\frac{2 \cdot L_2 \cdot X_2}{R_L}\right) \]
\[ X_6 = \sqrt{\frac{1}{(L_K \cdot C_S) - (R_S / (2 \cdot L_K))^2}} \]
\[ X_7 = \arctan\left(\frac{2 \cdot L_XS \cdot X_6}{R_Z + R_S}\right) \]
\[ W_0 = \sqrt{\frac{1}{(C_S \cdot (L_C + L_XS + L_XE + L_XF) + L_XS \cdot C_S - (R_Z + R_S) / (2 \cdot (L_XS + L_S)))^2}} \]
\[ W_1 = \sqrt{\frac{1}{(L_XS + L_S) \cdot C_S}} \]
\[ W_2 = \sqrt{\frac{1}{(L_1 \cdot C_S)}} \]

N=1  ! DATA MATRIX COEFFICIENT  
K=1  ! CYCLE NUMBER  
JL=1  ! LOW LEVEL CURRENT CYCLE COUNTER  
J=1  ! HIGH LEVEL CURRENT CYCLE COUNTER  
TFALL=0.0  ! SET HIGH TO LOW LEVEL TRANSITION TIME TO 0.0  
KPD=0  ! KPD DEFINES PERIOD AT END OF PREVIOUS CYCLE  
TRISE=1/F  ! SET MINIMUM LOW TO HIGH TRANSITION TIME  
ERRA=HILREF  ! SET INITIAL CURRENT ERROR TO MAXIMUM  
TW4=0.85*1.0E+06/F  ! SET INITIAL PULSE WIDTH TO 85% OF DEMAND  
OP1=0.0  ! INITIAL LOAD CURRENT  

*****
**PULSE WIDTH AND FREQUENCY DETERMINATOR SUBROUTINE**

* THE PULSE WIDTH (TPW) AND FREQUENCY (FO) ARE VARIED
* BY THIS ROUTINE IN ACCORDANCE WITH A SET OF RULES
* GOVERNING THE CLOSED LOOP CONTROL OF CURRENT IN THE
* ARC LOAD.
* POSITIVE CURRENT ERRORS (IREF>IF/B) AND NEGATIVE
* CURRENT ERRORS (IREF<IF/B) ARE POSSIBLE DUE TO THE
* LAG IN SYSTEM RESPONSE (<1 MILLISECOND) TO A CHANGE
* IN DEMANDED CURRENT AND/OR CHANGE IN ARC LOAD CONDITIONS
* WHICH CAN OCCUR IN < 100 MICROSECONDS.

44  
TF0=1/F
TF=FO
TMAX=0.85*TF0*1.0E+06 ! 85% OF TF0!
TMIN=6.0 ! MINIMUM TPW = 6.0 MICROSECONDS!

* IF LOAD RESISTANCE TOO HIGH FOR DEMANDED IREF....!
IF((HILREF-VI/RL).GT.0.0)THEN
TPW=TMAX
GO TO 40
ELSE
TPWSS=(HILREF*RL+VL)*TF0*1.0E+06/VI
END IF
ERROR=(HILREF-OP1)/50.0 ! ERROR (AMPS) TO VOLTS!
IF(ERROR.GT.1.0)THEN
TPW=TMAX
GO TO 40
END IF
IF(ERROR.GT.-0.1)THEN
TPW=TPWSS+ERROR*19
FO=F*TPW/6.0
GO TO 40
END IF
IF(ERROR.LE.-0.1)THEN
TPW=6.0
FO=15.0E+03+ERROR*3.0E+03 ! VARIABLE FREQUENCY!
GO TO 40
END IF

40 IF(TPW.GT.TMAX)TPW=TMAX
IF(TPW.LT.TMIN)TPW=TMIN
IF(FO.GT.15.0E+03)FO=15.0E+03 ! 15 KHZ MAXIMUM!
TPW=1/FO
TOFF=FO

* SET ALL VARIABLES TO INITIAL CONDITIONS
KWS=0
KW=0
ITM=0.0
IFM=0.0
UCEM=0.0
IF(NWRITE.EQ.0)THEN
WRITE(5,4300)

4300 FORMAT(//,1X,'J FO TKS ITM IFM UCEM OPV
- TR-TF PS OP1 TJ TJD PTRAN PD10DE EFF')
ELSE
GO TO 999
END IF

******
**** POWER MODULE SIMULATOR SUBROUTINE ****

PERIOD 1 EQUATIONS (FLYWHEEL DIODE FORWARD CURRENT TERMINATION)

QR=QD*(1+IL(K)/200.0) ! RECOVERED CHARGE AS FUNCTION OF ILOAD !
UT=UTR*(1+IL(K)/HILREF) ! TRANSISTOR VSAT AS FUNCTION OF ILOAD !
UF=UD*(1+IL(K)/HILREF) ! DIODE VOLT DROP AS FUNCTION OF ILOAD !
PRFD=QR*VI*FO ! DIODE FORWARD RECOVERY LOSS !
PLOSS=2.5*IL(K) ! TRANSFORMER,RECTIFIER,AUXILIARY SUPPLIES LOSSES !

RESET LOSSES TOTALISERS
PLD=0 ! TOTAL LOAD POWER !
PFD=0 ! FLYWHEEL DIODE LOSS !
PSR=0 ! SNUBBER LOSS !
PTR=0 ! TOTAL TRANSISTOR LOSSES !

K=0
IF(IL(K)>7.7,7,8 ! IF LOAD CURRENT = 0.0 SKIP PERIODS 1,2,3 !
IC(K)=0.0
IF(K)=0.0
IS(K)=0.0
IT(K)=0.0
IZ(K)=0.0
UCE(K)=VI
UL(K)=0.0
US(K)=VI
TK1=0.0
TK2=0.0
TK3=0.0
GO TO 11 ! GO TO PERIOD 4 !

DO 50 NT=1,75000,250 ! TIME INCREMENTS OF 0.25 MICROSECONDS !
    T=(NT-1)*1.0E-09
    N=ABS((NT-1)/250)+K+1

    IF(KPD.EQ.0)GO TO 3
    IF(KPD.EQ.6)GO TO 4
    IF(KPD.EQ.7)GO TO 4
    IF(KPD.EQ.8)GO TO 10
    IF(KPD.EQ.9)GO TO 5
    IF(KPD.EQ.90)GO TO 4

KPD=6,CCS STILL CHARGING (US<VZ)
ISZ(N)=IS(K)*COS(WX*T)-(US(K)*SIN(WX*T))/(WX*^2)*LXS)
IS(N)=ISZ(N)
IF(IS(N).LT.0.1)THEN
    KPD=0
    IS(N)=0.0
END IF

US(N)=-(US(K)/(WX**2*LXS*CS))*(COS(WX*T)-1)-(IS(K)/(WX*CS))*
   SIN(WX*T)-US(K))
US(L)=US(N)
IST(N)=0.0
IZ(N)=0.0
GO TO 6
KPD = 7: CS CHARGING THROUGH DZ, DZ CONDUCTING
EQUATIONS AS FOR KPD = 6

KPD = 8: DZ ONLY CONDUCTING
CURRENT TRANSFERS IMMEDIATELY TO TRANSISTOR
SNUBBER DISCHARGE COMMENCES
IZ(N) = 0.0
GO TO 3

KPD = 9: SNUBBER DISCHARGING THROUGH DF
5
KU = 1
KUS = 1
IC(N) = -(V1/RZ + (V1/RZ - IS(K)) * EXP(-RZ*T/L1))
IF(IZ(N) .GT. 0.1) THEN
KPD = 0
KU = 0
END IF
GO TO 3

IF CS WAS CHARGING, EQUATIONS AS FOR KPD = 6, 7
US(L) = US(K)
IST(N) = -(US(L) - UT) * SIN(X3*T) * EXP(-RS*T/(2*L3))/ (L3*X3)
+ KUS * IS(K) * COS(X3*T)
IF(IST(N) .GT. 0.0) THEN
IS(N) = 0.0
KE = 1
ELSE
IS(N) = IST(N)
END IF
US(N) = -(US(L) - UT)/X3 * (X3 - SQRT((1/(L3*CS))) * EXP(-RS*T/(2*L3)) * 
SIN(X3*T + X4) + US(L) + KU * IS(K) * SIN(X3*T)/(CS*X3)

IF(N) = IF(K) - ((-UT - VI + UF)/(LXF + LXE + LC)) * T
IL(N) = IL(K)
IF(KU .EQ. 1) THEN
IT(N) = -IS(N)
ELSE
IC(N) = IL(N) - IF(N) + IC(K)
IT(N) = IC(N) - IS(N)
END IF
IZ(N) = 0.0
IF((1 - T/TR).LT.0.1) THEN
UCE(N) = UT
ELSE
UCE(N) = UCE(N - 1) * (1 - T/TR)
END IF
UL(N) = VL + IL(N) * RL

PT(N) = IT(N) * UCE(N)
PTR = PTR + PT(N)
PF(N) = ABS(IF(N) * UF)
PFD = PF + PF(N)
IF(IS(N) .LT. 0.0) THEN
PS(N) = ABS(IS(N) * 2*RS)
ELSE
PS(N)=0.0
PSR=PSR+PS(N)
END IF
PL(N)=IL(N)*UL(N)
PLD=PLD+PL(N)
*
*
SAVE PEAK VALUES!
TP=T*1.0E+06
IF(UCE(N).GT.UCEM)UCEM=UCE(N)
IF(IT(N).GT.ITM)ITM=IT(N)
IF(IF(N).GT.IFM)IFM=IF(N)
IF(IF(N))9,9,50
50 CONTINUE
9 M1=N
ERR=HILREF-IL(M1)
T1=-IF(1)*(LXF+LXE+LC)/(UT-V1-UF)
TK1=T
KPD=1
KP=N.
*
*
*****
* PERIOD 2 EQUATIONS (FLYHEEL DIODE FORWARD RECOVERY)

* TIME SHIFT T BY T1
DO 60 NT=1,75000,250
T=(NT-1)*1.0E-09+TK1+250.0E-09
N=ABS((NT-1)/250)+M1+1

* DIF=ABS(-UT+VI+UF)/(LXF+LXE+LC)
TFR=SQR((3*OR/((1+S)*DIF)) ! FORWARD RECOVERY TIME !

13 IST(N)=-(US(K)-UT)*SIN(X3*T)*EXP(-RS*T/(2*L3)))/L3*X3)
-+KW*IS(K)*COS(X3*T)
IF(IST(N).GT.0.0)THEN
IS(N)=0.0
KS=1 ! INITIAL SNUBBER DISCHARGE COMPLETE ! ELSE
IS(N)=IST(N)
IF(KS.EQ.1)IS(N)=0.0
END IF

IF(N)=IF(K)-((-UT+VI+UF)/(LXF+LXE+LC))*T
IL(N)=((VI-UL(K))*(T-TK1)/LF)+IL(K)
IC(N)=IL(N)-IF(N)
IT(N)=IC(N)-IS(N)
IZ(N)=0.0

UCE(N)=UT
UL(N)=WL+IL(N)*RL
US(N)=-(US(K)-UT)/X3)*(X3-SQR((1/(L3*CS)))*EXP(-RS*T/(2*L3)))*
- SQR((1/(L3*CS)))*EXP(-RS*T/(2*L3))

PT(N)=IT(N)*UCE(N)
PTR=PTR+PT(N)
PF(N)=ABS(IF(N)*UF)
PFD=PFD+PF(N)
IF(IS(N).LT.0.0)THEN
PS(N)=ABS(IS(N)**2*RS)
ELSE
PS(N)=0.0
END IF
PSR=PSR+PS(N)
PL(N)=IL(N)*UL(N)
PLD=PLD+PL(N)

TP=T*1.0E+06

IF(UCE(N).GT.UCEM)UCEM=UCE(N)
IF(IT(N).GT.ITM)ITM=IT(N)
IF(IF(N).GT.1FM)IFM=IF(N)
IF(T.GT.(T1+TFR)) GO TO 15

60 CONTINUE
15 T2=T1+TFR
M2=N
ERR=HILREF-IL(M2)
TK2=T
IF(M2)=IF(N)
KPD=2
KP=N

*****
PERIOD 3 EQUATIONS (FLYWHEEL DIODE REVERSE RECOVERY)

TIME SHIFT T BY T2
DO 70 NT=1,7500,250
T=(NT-1)*1.0E-09+TK2+250.0E-09
N=ABS((NT-1)/250)+M2+1

IST(N)=-((US(K)-UT)*SIN(X3*T)*EXP(-RS*T/(2*L3)))/(L3*X3)
+KWS*IS(K)*COS(X3*T)
IF(IST(N).GT.0.0)THEN
IS(N)=0.0
KS=1
ELSE
IS(N)=IST(N)
IF(KS.EQ.1)IS(N)=0.0
END IF

A=(T-T2)/(S*TFR)
IF(N)=IF(M2)*(1-A)
IF(IF(N).GT.-0.1)THEN
IF(N)=0.0
KF=1 ! FLYWHEEL DIODE RECOVERY COMPLETE !
END IF

IL(N)=((VI-UL(K))*(T-TK1)/LF)+IL(K)
IC(N)=IL(N)-IF(N)
IT(N)=IC(N)-IS(N)
IZ(N)=0.0

UCE(N)=UT
UL(N)=UL+IL(N)*RL
US(N)=-(US(K)-UT)*X3*(X3-SQRT((1/(L3*CS)))*EXP(-RS*T/(2*L3)))+US(K)

PT(N)=IT(N)*UCE(N)
PTR=PTR+PT(N)
PF(N)=ABS(IF(N)*UF)
PFD=PF0+PF(N)
IF(IS(N).LT.0.0)THEN
PS(N)=ABS(IS(N)**2*RS)
ELSE
PS(N)=0.0
END IF

PSR=PS+PSR(N)
PL(N)=IL(N)*UL(N)
PLD=PLD+PL(N)

TP=T*1.0E+06
IF(UCE(N).GT.UCEM)UCEM=UCE(N)
IF(IT(N).GT.ITM)ITM=IT(N)
IF(IF(N).GT.IFM)IFM=IF(N)
IF(KF.EQ.1)GO TO 19
70 CONTINUE
19 M3=N
ERR=HILREF-IL(M3)
TK3=T
KPD=3
KP=N

*****
PERIOD 4 EQUATIONS (TRANSISTOR CONDUCTION)

TIME SHIFT T BY T3

1. \( \text{LPW} = \text{IFIX}(\text{TPW}) \)
2. \( \text{LPWM} = \text{LPW} \times 1000 \) PULSE WIDTH IN 0.25 MICROSECOND STEPS
3. \( \text{DO 80 NT}=1, \text{LPWM}, 250 \)
4. \( T=(\text{NT}-1) \times 1.0E-09 + \text{TK3} + 250.0E-09 \)
5. \( \text{IF}(T \lt \text{LPW} \times 1.0E-06) \text{GO TO 1} \) TIME > PULSE WIDTH
6. \( \text{N} = \text{ABS}((\text{NT}-1) / 25D) + \text{M} + 1 \)
7. \( \text{KL} = 0 \)
8. \( \text{IL}(N) = ((\text{VI}-\text{UL}(K)) \times (T-\text{TK1}) / \text{LF}) + \text{IL}(K) \)
9. \( \text{IF}(\text{IL}(N) \lt \text{HILREF} \times 1.010) \text{KL} = 1 \) 1% ERROR
10. \( \text{IC}(N) = \text{IL}(N) \)
11. \( \text{IF}(N) = 0.0 \)
12. \( \text{IZ}(N) = 0.0 \)

IF (KS.EQ.0) GO TO 23 SNUBBER IN INITIAL DISCHARGE
IF (KS.EQ.1) GO TO 20 SNUBBER DISCHARGING WITH US<UT
IF (KS.EQ.2) GO TO 22 SNUBBER DISCHARGING THRU DZ
IF (KS.EQ.3) GO TO 12 SNUBBER DISCHARGES THRU TRANSISTOR

INITIAL SNUBBER DISCHARGE

13. \( \text{IST}(N) = -((\text{US}(K) - \text{UT}) \times \text{SIN}(X3 \times T) \times \text{EXP}(-\text{RS} \times T / (2 \times \text{L3})) / (\text{L3} \times X3) \)
14. \( + \text{KWS} \times \text{IS}(K) \times \text{COS}(X3 \times T) \)
15. \( \text{US}(N) = -((\text{US}(K) - \text{UT}) / X3) \times (X3 - \text{SQRT}((1 / (\text{L3} \times \text{CS}))) \times \text{EXP}(-\text{RS} \times T / (2 \times \text{L3})) \)
16. \( \times \text{SIN}(X3 \times T + X4) + \text{US}(K) \)
17. \( \text{USL} = \text{US}(N) \)
18. \( \text{IF}(\text{USL} \leq \text{UT}) \text{THEN} \)
19. \( \text{US}(N) = \text{UT} \)
20. \( \text{KS} = 1 \)
21. \( \text{END IF} \)
22. \( \text{IS}(N) = \text{IST}(N) \)
23. \( \text{ISN} = \text{IS}(N) \)
24. \( \text{TSO} = T \)
25. \( \text{KWS} = 0 \)
26. \( \text{IT}(N) = \text{IC}(N) - \text{IS}(N) \)
27. \( \text{GO TO 21} \)

KS=1, WHEN US<UT; LS SELF DISCHARGES; LXS CONTINUES TO DISCHARGE

28. \( \text{ISL}(N) = \text{ISN} \times \text{EXP}(-\text{RS} \times (T-\text{TSO}) / \text{LS}) \)
29. \( \text{IF}(\text{ISL}(N) \lt \text{UT} \times 0.1) \text{THEN} \)
30. \( \text{ISL}(N) = 0.0 \)
31. \( \text{END IF} \)
32. \( \text{ISM}(N) = \text{ISN} \times \text{COS}(\text{WX} \times (T-\text{TSO})) \)
33. \( \text{US}(N) = (\text{ISN} / (\text{WX} \times \text{CS})) \times \text{SIN}(\text{WX} \times (T-\text{TSO})) \)
34. \( \text{IF}(\text{ISM}(N) \lt \text{UT} \times 0.1) \text{THEN} \)
35. \( \text{ISM}(N) = 0.0 \)
36. \( \text{KS} = 2 \)
37. \( \text{END IF} \)
38. \( \text{USM} = \text{US}(N) \)
39. \( \text{IF}(\text{USM} \leq \text{UT}) \text{US}(N) = \text{UT} \)
40. \( \text{TSI} = T \)
41. \( \text{IS}(N) = \text{ISM}(N) \)
42. \( \text{IT}(N) = \text{IC}(N) - \text{IS}(N) \)
43. \( \text{GO TO 21} \)

CS BEGINS TO DISCHARGE RESONANTLY THRU DZ; ISL(N) ALSO CONTINUES
ISP(N) = -(USM/(WX*LXS))*SIN(WX*(T-TS1))
ISL(N) = ISN*EXP(-R5*(T-TS0)/LS)
IF(ISP(N).LT.-0.1)THEN
KS=3
ISP(N)=0.0
END IF
TS2=T
ISK=ISL(N)
IS(N)=ISP(N)
US(N)=USM*COS(WX*(T-TS1))
USP=US(N)
IF(USP.LE.UT)US(N)=UT
IT(N)=IC(N)
GO TO 21

KS=3; CS DISCHARGES THRU TRANSISTOR TILL US<UT

IST(N) =-((USP-UT)*SIN(X3*(T-TS2))*EXP(-RS*(T-TS2)/(2*L3)))
US(N) =-((USP-UT)/X3)*(X3-SQRT((1/(L3*CS)))*EXP(-RS*(T-TS2))
- (2*L3))*SIN(X3*(T-TS2)+X4)+USP
GO TO -14

21 UL(N) = VL+RL*IL(N)
UCE(N) = UT

PT(N) = IT(N)*UCE(N)
PTR=PTR+PT(N)
PF(N) = ABS(IF(N)*UF)
PFD=PFD+PF(N)
IF(IS(N).LT.0.0)THEN
PS(N) = ABS(IS(N)**2*RS)
ELSE
PS(N) = 0.0
END IF
PSR=PSR+PS(N)
PL(N) = IL(N)*UL(N)
PLD=PLD+PL(N)

TP=T*1.0E+06

 IF(UCE(N).GT.UCEM)UCEM=UCE(N)
 IF(IT(N).GT.IM)ITM=IT(N)
 IF(IF(N).GT.IM)IFM=IF(N)
 IF(KL.EQ.1)GO TO 1
80 CONTINUE
1 M4=N
ERR=HILREF-IL(M4)
T4=T3+NT*1.0E-06
TK4=T
KPD=4
KP=N

******
PERIOD 5 EQUATIONS (TRANSISTOR CURRENT FALL TIME)

TIME SHIFT T BY T4
DO 90 NT=1,75000,250
T=(NT-1)*1.0E-09+TK4+250.0E-09
N=ABS((NT-1)/250)+M4+1

IL(N)=IL(M4)
IC(N)=IC(M4)
IT(N)=IT(M4)*EXP(-5.0*(T-TK4)/TF)
IF(IT(N).GT.0.25)GO TO 28
IT(N)=0.0
IS(N)=IL(N)
GO TO 26

28 IF(IS(M4))24,24,25
24 ISL(N)=IT(M4)-IT(N)
IS(N)=ISL(N)
GO TO 26

25 ISL(N)=IT(M4)-IT(N)+IS(M4)
IS(N)=ISL(N)
26 IF(N)=0.0
IZ(N)=0.0
UL(N)=UL(M4)
US(N)=US(M4)+(1/CS)*((T-TK4)*((IT(M4)+IS(M4))+(TF/5)*IT(M4)*EXP(-5*(T-TK4)/TF))-1)
UCE(N)=US(N)+LXS*IT(M4)*(5/TF)*EXP(-5*(T-TK4)/TF)

PT(N)=IT(N)*UCE(N)
PTR=PTR+PT(N)
PF(N)=ABS(IF(N)*UF)
PFD=PFD+PF(N)
IF(IS(N).LT.0.0)THEN
PS(N)=ABS(IS(N)**2*RS)
ELSE
PS(N)=0.0
END IF
PSR=PSR+PS(N)
PL(N)=IL(N)*UL(N)
PLD=PLD+PL(N)

TP=T*1.0E+06
IF(UCE(N).GT.UCEM)UCEM=UCE(N)
IF(IT(N).GT.1M)ITM=IT(N)
IF(IF(N).GT.1M)IFM=IF(N)
IF(IT(N).LT.0.1)GO TO 27
90 CONTINUE
27 MS=N
ERR=HILREF-IL(MS)
IT(N)=0.0
TS=T4+TF
KPD=S
TK5=T
KP=N
PERIOD 6 EQUATIONS (INDUCTIVE ENERGY DUMPING INTO CS)

* TIME SHIFT T BY T5
  KZ=0
  KS=0
  DO 100 NT=1,75000,250
  T=(NT-1)*1.0E-09+TK5+250.0E-09
  N=ABS((NT-1)/250)+M5+1

* IF(T.GT.TOFF)THEN ! GO TO NEXT CYCLE PERIOD 1 !
  KP=N
  GO TO 39
  END IF

* ASSUME THAT SNUBBER CHARGING CONTINUES; ISL(N)>0
  THEN TEST FOR UCE(N)>VZ
  IF(IS(N-1).LT.0.1) THEN
    TK7=T
    TK8=T
    M7=N
    M8=N
    UL(N)=UL(N-1)
    USF=US(N-1)
    US(N)=US(N-1)
    IL(N)=IL(N-1)
    UCE(N)=US(N-1)
  END IF

  IF(UCE(N).LT.VI) THEN
    KS=2
  ELSE
    KS=3
  END IF
  GO TO 29
  END IF

31 IC(N)=IL(M5)*COS(W0*(T-TK5))
  IF(IC(N).LT.0.1) THEN
    IC(N)=0.0
    IS(N)=IC(N)
    KS=2
  END IF
  I5(N)=IC(N)
  UCE(N)=US(M5)+(IL(M5)*SIN(W0*(T-TK5)))*((1/(CS*WO)-WO*LXS))/
  US(N)=US(M5)+(IL(M5)*SIN(W0*(T-TK5)))/(CS*WO))
  IF(UCE(N).GT.UCEM) UCEM=UCE(N)
  IF(ABS(UCE(N)).GT.VZ) THEN ! ZENER DIODE CONDUCTING!
    KZ=1
  END IF

33 UCE(N)=VZ
  END IF

* IL(N)=-(USF+VL)/RL+(IL(M5)+(USF+VL)/RL)*EXP(-RL*(T-TK5))/
  (2*(LXF+LF)))
  IF(N).LT.IL(N)-IC(N)
  IZ(N)=0.0
  IT(N)=0.0
  UL(N)=VL+IL(N)*RL
PT(N) = IT(N) * UCE(N)
PTR = PTR + PT(N)
PF(N) = ABS(IF(N) * UF)
PFD = PFD + PF(N)
IF(IS(N) .LT. 0.0) THEN
  PS(N) = ABS(IS(N) ** 2 * RS)
ELSE
  PS(N) = 0.0
END IF
PSR = PSR + PS(N)
PL(N) = IL(N) * UL(N)
PLD = PLD + PL(N)

TP = T * 1.0E+06
IF(IF(N) .GT. IFM) IFM = IF(N)
IF(KZ .EQ. 1) G0 TO 29 ! GO TO PERIOD 7 !
T6 = T
100 CONTINUE
29 M6 = N
ERR = HILREF - IL(M6)
TK6 = T
US(M6) = US(N)
ICZ = IC(M6)
KPD = 6
KP = N

IF IC = 0: SKIP PERIODS VII, VIII

IF(KZ .EQ. 1) G0 TO 35
IF(KS .EQ. 2) G0 TO 41
IF(KS .EQ. 3) G0 TO 41

*****
**PERIOD 7 EQUATIONS (ZENER CURRENT INCREASING FROM ZERO)**

[OCCURS ONLY IF UCE>VZ IN PERIOD VI]

TIME SHIFT T BY T6

35

K7=0
DO 110 NT=1,75000,250
T=(NT-1)*1.0E-09+TK6+250.0E-09

IF(T.GT.TOFF)THEN
KP=N
GO TO 39
END IF
N=ABS((NT-1)/250)+M6+1

RQ=RZ+RS
LQ APPROXIMATED BY DIVIDING BY A NUMBER (3) TO GET RESULT
THIS IS NECESSARY DUE TO DIFFICULTY IN ESTIMATING THE
STRAY INDUCTANCE IN THE POWER MODULE CIRCUIT

LQ=(LXS+LS)/3
IC(N)=(VI-VZ)/RZ+(ICZ-(VI-VZ)/RZ)*EXP(-RZ*(T-TK6)/(LC+LXE+LXF))
ISZ(N)=(ICZ-(T-TK6)*US(M6)*2-ICZ*RQ)/(2*LQ)+EXP(-RQ*(T-TK6)/(2*LQ))
XQ=SQR((1/(CS*LQ))-(RQ/(2*LQ))^2)
IS(N)=ISZ(N)
IF(IS(N).LT.0.1) THEN
IS(N)=0.0
K7=1  SNUBBER CURRENT TRANSFERRED TO LOAD AND ZENER!
IZ(N)=IC(N)
GO TO 36
END IF
IZ(N)=IC(N)-ISZ(N)

36
IL(N)=-(UF+VL)/RL+(IL(M5)+(UF+VL)/RL)*EXP(-RL*(T-TK5)/(2*(LXF+LF)))
IF(N)=IL(N)-IC(N)
IT(N)=0.0
UL(N)=VL+RL*IL(N)

AK0=1/CS
AK1=RQ/(2*LQ)
AK2=ICZ
AK3=(2*US(M6)-ICZ*RQ)/(2*LQ)
US(N)=(AK0/AK1)*((AK3*(T-TK6)+AK3/AK1-AK2)*EXP(-AK1*(T-TK6))-
(AK3/AK1-AK2)+US(M6))
UCE APPROX. US(N) AS MEASURED VALUE INCLUDES LXE IN CIRCUIT
UCE(N)=US(N)

PT(N)=IT(N)*UCE(N)
PTR=PTR+PT(N)
PF(N)=ABS(IF(N)*UF)
PFD=PFD+PF(N)
IF(IS(N).LT.0.0) THEN
PS(N)=ABS(IS(N)**2*RS)
ELSE
PS(N)=0.0
END IF
PSR=PSR+PS(N)
PL(N) = IL(N) * UL(N)
PLD = PLD + PL(N)

* TP = T * 1.0E+06
IF (UCE(N) .GT. UCEM) UCEM = UCE(N)
IF (IF(N) .GT. IFM) IFM = IF(N)
IF (K7 .EQ. 1) GO TO 34

110 CONTINUE
34 T7 = T
M7 = N
ERR = HILREF - IL(M7)
TK7 = T
US(M7) = US(N)
KPD = 7

*
KP = N
*
*
*
****
**PERIOD 8 EQUATIONS (ZENER CURRENT DECREASING TO ZERO)**

[OCCURS ONLY IF UCE > VZ IN PERIOD VI]

**TIME SHIFT T BY T7**

K8 = 0
LPC = 0

DO 120 NT = 1, 75000, 250
T = (NT-1)*1.0E-09 + TK7 + 250.0E-09

IF (T.GT.TOFF) THEN
KP = N
GO TO 39
END IF
N = ABS((NT-1)/250) + M7 + 1

IC(N) = (VI-VZ)/RZ + (IFZ-(VI-VZ)/RZ) * EXP(-RZ*(T-TK6)/(LC+LXE+LXF))
IF (IC(N).LT.0.0) THEN
IC(N) = 0.0
LPC = 1
END IF

IZ(N) = IC(N) - IS(N)
IF (IZ(N).LE.0.0) THEN
IZ(N) = 0.0
K8 = 1 ! ZENER CURRENT CEASES TO FLOW!
END IF

IL(N) = -(UF+VL)/RL + (IL(M5)+(UF+VL)/RL) * EXP(-RL*(T-TK5)/(2*(LXF+LF)))
IT(N) = 0.0
UL(N) = VL + RL * IL(N)

ASSUME CS DISCHARGE COMMENCES IN PERIOD IX
US(N) = US(N-1)
UCE(N) = UCE(N)
IS(N) = 0.0

PT(N) = IT(N) * UCE(N)
PTR = PTR + PT(N)
PF(N) = ABS(IF(N) * UF)
PFD = PFD + PF(N)
IF (IS(N).LT.0.0) THEN
PS(N) = ABS(IS(N)**2*RS)
ELSE
PS(N) = 0.0
END IF
PSR = PSR + PS(N)
PL(N) = IL(N) * UL(N)
PLD = PLD + PL(N)

TP = T*1.0E+06
IF (UCE(N).GT.UCEM) UCEM = UCE(N)
IF (IF(N).GT.IFM) IFM = IF(N)
IF (LPC.EQ.1) GO TO 37
120 CONTINUE
37 T8 = T
MB = N
ERR = HILREF - IL(M8)
TK8 = T
USF = US(N)
KPD = 0
KP = N
KS = 0
PERIOD 9 EQUATIONS (FLYWHEEL OF LOAD CURRENT)

TIME SHIFT T BY T8 IF UCE(P6)>VZ

41
TS3=T
DO 130 NT=1,75000,250
T=(NT-1)*1.0E-09+TK8+250.DE-09

IF(T.GT.TOFF)THEN
KP=N-1
GO TO 39
END IF
N=ABS((NT-1)/250)+MB+1

IF(KS.EQ.3)GO TO 16
IF(KS.EQ.0)GO TO 16
IF(KS.EQ.1)GO TO 17
IF(KS.EQ.2)GO TO 18

INITIAL SNUBBER DISCHARGE

16
KPD=9
ISF(N)=-(US(M8)-VI)*SIN(XK*(T-TK8))*EXP(-RS*(T-TK8)/(2*LK)))/
(LK*XK)
US(N)=-(US(M8)-VI)/XK)*(XK-SQRT(1/((LJ*CS)))*EXP(-RS*(T-TK8))/
(2*LK))*SIN(XK*(T-TK8)+X0)+US(MB)
32
USL=US(N)
IF(USL.LE.VI)THEN
KS=1
END IF
IS(N)=ISF(N)
ISN=IS(N)
IC(N)=IS(N)
TS0=T
KWS=0
GO TO 43

KS=1, WHEN US<VI; LS SELF DISCHARGES; LXS CONTINUES TO DISCHARGE

17
KPD=9
ISL(N)=ISN*EXP(-RS*(T-TS0)/LS)
IF(ISL(N).GT.-0.1) THEN
ISL(N)=0.0
END IF
ISM(N)=ISN*COS(WZ*(T-TS0))
US(N)=(ISN/(WX*CS))*SIN(WX*(T-TS0))+VI
IF(ISM(N).GT.-0.1) THEN
ISM(N)=0.0
KS=2
END IF
USM=US(N)
TS1=T
IS(N)=ISM(N)
IC(N)=IS(N)
GO TO 43

US(N)=US(N-1)
\[ IS(N) = 0.0 \]
\[ KPD = G \]
\[ IC(N) = IS(N) \]
GO TO 43

* 43  
\[ UCE(N) = IS(N) \]
\[ IL(N) = -(UF+VL)/RL + (IL(M5)+(UF+VL)/RL) \times \exp\left(-RL \times (T-TK5)/(2 \times (LF+LF))\right) \]
\[ IF(N) = IL(N) - IC(N) \]
\[ IZ(N) = G.a \]
\[ IT(N) = G.D \]
\[ UL(N) = VL + IL(N) \times RL \]
\[ PT(N) = IT(N) \times UCE(N) \]
\[ PTR = PTR + PT(N) \]
\[ PF(N) = \text{ABS}(IF(N) \times UF) \]
\[ PFD = PFD + PF(N) \]
\[ IF(15(N) \times LT.D.G) \text{THEN} \]
\[ PS(N) = \text{ABS}(IS(N) \times 2 \times RS) \]
\[ \text{ELSE} \]
\[ PS(N) = 0.0 \]
\[ \text{END IF} \]
\[ PSR = PSR + PS(N) \]
\[ PL(N) = IL(N) \times UL(N) \]
\[ PLD = PLD + PL(N) \]
\[ TP = T \times 1.0E+06 \]
\[ \text{IF}(UCE(N) \times GT. UCEM) \text{UCEM} = UCE(N) \]
\[ \text{IF}(IF(N) \times GT. IFM) \text{IFM} = IF(N) \]
130 CONTINUE
39 M9 = N
\[ ERR = HILREF - IL(M9) \]
\[ TK9 = T \]
\[ KP = N \]

PLOAD = PLD \times 250.0E-09/TOFF
\[ TIME = 250.0E-09/TOFF \]
\[ PTRAN = PTR \times TIME \]
\[ PSNUB = PSR \times TIME \]
\[ PDIODE = (PFD + PDIODE) \times TIME \]
\[ ZLOSS = PTRAN + PSNUB + PDIODE + PLOSS \]
\[ PTOT = ZLOSS + PLOAD \]

\[ RIPPLE = IL(M4) - IL(M9) \] \text{RIPPLE CURRENT EVALUATION !}
\[ EFF = 100 \times \text{PLOAD} / (\text{PLOAD} + ZLOSS) \] \text{EFFICIENCY (%) !}

RCA = RCH + RHA \text{ CASE TO AMBIENT THERMAL RESISTANCE OF TRANSISTORS !}
RJA = TRJC + RCA \text{ JUNCTION TO AMBIENT THERMAL RESISTANCE OF TRANSISTOR !}
RCAD = RCHD + RHAD \text{ CASE TO AMBIENT THERMAL RESISTANCE OF DIODE !}
RJAD = DJC + RCAD \text{ JUNCTION TO AMBIENT THERMAL RESISTANCE OF DIODE !}

TAMB = 0.005 \times ZLOSS + TA \text{ INCREASE AMBIENT WITHIN MODULE ENCLOSURE !}
\[ TC = \text{(PTRAN} \times 1.25/\text{NTRAN}) \times RCA + \text{TAMB} \] \text{TRANSISTOR CASE TEMPERATURE !}
\[ TJ = \text{(PTRAN} \times 1.25/\text{NTRAN}) \times RJA + \text{TAMB} \] \text{TRANSISTOR JUNCTION TEMPERATURE !}
\[ TCD = PDIODE \times RCAD + TAMB \] \text{DIODE CASE TEMPERATURE !}
\[ TJD = PDIODE \times RJAD + TAMB \] \text{DIODE JUNCTION TEMPERATURE !}

OP1 = 0.5 \times (IL(M9) + IL(M4)) \text{ CALCULATE AVERAGE OUTPUT CURRENT !}
OPV = VL + OP1 \times RL \text{ OUTPUT VOLTAGE !}
ERRA=HILREF-0.5*(IL(M9)+IL(M5)) ! CALCULATE CURRENT ERROR!

IF(J.GT.14)GO TO 45 ! SWITCH REFERENCE FROM HIGH TO LOW!
IF(ABS(ERRA).GT.HILREF*0.05) THEN
TRISE=KP*250.0E-09 ! CALCULATE RISE TIME!
ELSE
TRISE=TRISE
END IF
45 WRITE(5,4200)J,FO,TK4,ITM,IFM,UCEM,OPV,TRISE,PSNUB,-OPI,TJ,TJD,PTRAN,PDIODE,EFF
4200 FORMAT(I2,2E9.2,4F7.2,E10.2,F7.1,F7.1,2F6.1,E10.2,E10.2,F7.1)

J=J+1 ! INCREMENT FOR NEXT CYCLE!
K=KP
NWRITE=1
IF(J.LT.15) THEN
GO TO 44 ! CONTINUE HIREF CYCLES!
ELSE
HILREF=BILREF ! CHANGE TO LOW REFERENCE CURRENT!
END IF

IF(ABS(HILREF-OPI).GT.5.0) THEN
TFALL=TFALL+1.0/FO ! FALL TIME TOTALISER!
ELSE
TFALL=TFALL
END IF
TRISE=TFALL
IF(J.GT.50)GO TO 42 ! TERMINATE ROUTINE AFTER 50 CYCLES!

GO TO 44

CALL CONECT(0,5) ! CLOSE DATA FILES!
42 STOP
END
Effect of varying d.c. supply voltage $V_i$ (40 - 80 volts)
<table>
<thead>
<tr>
<th>J</th>
<th>F o</th>
<th>ILK</th>
<th>ILM</th>
<th>LFS</th>
<th>UCEN</th>
<th>UL</th>
<th>TR</th>
<th>RIP</th>
<th>ILK</th>
<th>LJ</th>
<th>TJD</th>
<th>TRAN</th>
<th>PD100E</th>
<th>V1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>78.8</td>
<td>29.0</td>
<td>35.8</td>
<td>16.1</td>
<td>0.30E-04</td>
<td>1.4</td>
<td>28.7</td>
<td>30.6</td>
<td>26.7</td>
<td>0.29E+02</td>
<td>0.43E+01</td>
<td>60.00</td>
</tr>
<tr>
<td>2</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>61.0</td>
<td>55.7</td>
<td>51.4</td>
<td>17.2</td>
<td>0.30E-03</td>
<td>1.4</td>
<td>54.0</td>
<td>56.8</td>
<td>28.3</td>
<td>0.63E+02</td>
<td>0.13E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>5</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>117.9</td>
<td>95.4</td>
<td>74.3</td>
<td>18.2</td>
<td>0.35E-03</td>
<td>1.5</td>
<td>80.5</td>
<td>66.8</td>
<td>61.3</td>
<td>0.12E+03</td>
<td>0.26E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>6</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>104.6</td>
<td>149.5</td>
<td>102.6</td>
<td>19.2</td>
<td>0.20E-03</td>
<td>1.5</td>
<td>105.0</td>
<td>57.8</td>
<td>34.0</td>
<td>0.17E+03</td>
<td>0.57E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>7</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>252.0</td>
<td>238.5</td>
<td>144.8</td>
<td>21.0</td>
<td>0.30E-03</td>
<td>1.7</td>
<td>150.4</td>
<td>82.3</td>
<td>44.0</td>
<td>0.30E+03</td>
<td>0.77E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>8</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>257.2</td>
<td>265.4</td>
<td>151.1</td>
<td>21.9</td>
<td>0.35E-03</td>
<td>1.8</td>
<td>171.7</td>
<td>92.6</td>
<td>46.4</td>
<td>0.36E+03</td>
<td>0.76E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>9</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>256.4</td>
<td>292.7</td>
<td>157.2</td>
<td>22.7</td>
<td>0.40E-03</td>
<td>1.8</td>
<td>192.2</td>
<td>103.6</td>
<td>53.1</td>
<td>0.42E+03</td>
<td>0.72E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>10</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>259.0</td>
<td>325.4</td>
<td>169.6</td>
<td>23.5</td>
<td>0.45E-03</td>
<td>1.8</td>
<td>211.8</td>
<td>113.8</td>
<td>58.0</td>
<td>0.47E+03</td>
<td>0.76E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>11</td>
<td>0.20E+05</td>
<td>0.39E-04</td>
<td>287.8</td>
<td>351.1</td>
<td>176.8</td>
<td>24.2</td>
<td>0.50E-03</td>
<td>1.9</td>
<td>230.6</td>
<td>126.3</td>
<td>63.0</td>
<td>0.54E+03</td>
<td>0.79E+02</td>
<td>60.00</td>
</tr>
<tr>
<td>12</td>
<td>0.20E+05</td>
<td>0.19E-04</td>
<td>280.7</td>
<td>385.1</td>
<td>186.3</td>
<td>25.0</td>
<td>0.50E-03</td>
<td>6.8</td>
<td>249.5</td>
<td>92.5</td>
<td>34.9</td>
<td>0.33E+03</td>
<td>0.53E+03</td>
<td>60.00</td>
</tr>
<tr>
<td>13</td>
<td>0.20E+05</td>
<td>0.15E-04</td>
<td>343.8</td>
<td>384.8</td>
<td>185.9</td>
<td>25.0</td>
<td>0.50E-03</td>
<td>7.5</td>
<td>246.9</td>
<td>86.5</td>
<td>37.9</td>
<td>0.30E+03</td>
<td>0.55E+03</td>
<td>60.00</td>
</tr>
<tr>
<td>14</td>
<td>0.20E+05</td>
<td>0.16E-04</td>
<td>343.8</td>
<td>387.4</td>
<td>188.9</td>
<td>25.0</td>
<td>0.50E-03</td>
<td>7.3</td>
<td>249.0</td>
<td>89.3</td>
<td>33.5</td>
<td>0.37E+03</td>
<td>0.53E+03</td>
<td>60.00</td>
</tr>
<tr>
<td>15</td>
<td>0.20E+05</td>
<td>0.16E-04</td>
<td>343.9</td>
<td>386.9</td>
<td>188.4</td>
<td>25.0</td>
<td>0.50E-03</td>
<td>7.4</td>
<td>249.0</td>
<td>88.6</td>
<td>33.8</td>
<td>0.31E+03</td>
<td>0.53E+03</td>
<td>60.00</td>
</tr>
</tbody>
</table>

Effect of varying the modulating (chopping) frequency $F_o$ (10-20kHz)
Transistor current fall time (Tf) variation
Transistor current fall time (Tf) variation
Transistor current fall time variation (0.5 - 3.0μS)
<table>
<thead>
<tr>
<th>J</th>
<th>F0</th>
<th>TK5</th>
<th>ITM</th>
<th>IFM</th>
<th>UCEM</th>
<th>OPG</th>
<th>TR-F</th>
<th>PS</th>
<th>QPI</th>
<th>TJ</th>
<th>IJD</th>
<th>PTRAN</th>
<th>PDIODE</th>
<th>EFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>53.49</td>
<td>50.14</td>
<td>53.73</td>
<td>10.93</td>
<td>10.85e-04</td>
<td>38.1</td>
<td>45.8</td>
<td>20.4</td>
<td>26.1</td>
<td>0.44e+02</td>
<td>0.37e+01</td>
<td>84.4</td>
</tr>
<tr>
<td>2</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>133.90</td>
<td>98.22</td>
<td>102.45</td>
<td>18.61</td>
<td>0.13e+03</td>
<td>35.8</td>
<td>90.2</td>
<td>39.7</td>
<td>29.0</td>
<td>0.12e+03</td>
<td>0.92e+01</td>
<td>82.0</td>
</tr>
<tr>
<td>3</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>252.70</td>
<td>134.79</td>
<td>149.94</td>
<td>20.13</td>
<td>0.20e+03</td>
<td>53.7</td>
<td>128.2</td>
<td>51.4</td>
<td>30.5</td>
<td>0.21e+03</td>
<td>0.17e+02</td>
<td>80.9</td>
</tr>
<tr>
<td>4</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>326.90</td>
<td>108.03</td>
<td>189.70</td>
<td>21.51</td>
<td>0.27e+03</td>
<td>43.5</td>
<td>162.7</td>
<td>43.8</td>
<td>33.3</td>
<td>0.51e+03</td>
<td>0.28e+02</td>
<td>81.6</td>
</tr>
<tr>
<td>5</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>355.13</td>
<td>220.78</td>
<td>213.24</td>
<td>22.76</td>
<td>0.33e+03</td>
<td>5.0</td>
<td>194.1</td>
<td>75.2</td>
<td>36.8</td>
<td>0.41e+03</td>
<td>0.46e+02</td>
<td>82.1</td>
</tr>
<tr>
<td>6</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>379.09</td>
<td>254.90</td>
<td>216.46</td>
<td>23.89</td>
<td>0.49e+03</td>
<td>1.2</td>
<td>222.2</td>
<td>86.3</td>
<td>42.3</td>
<td>0.50e+03</td>
<td>0.77e+02</td>
<td>82.1</td>
</tr>
<tr>
<td>7</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>502.24</td>
<td>234.77</td>
<td>263.89</td>
<td>24.90</td>
<td>0.47e+03</td>
<td>1.9</td>
<td>247.5</td>
<td>95.6</td>
<td>67.6</td>
<td>0.57e+03</td>
<td>0.97e+02</td>
<td>82.3</td>
</tr>
<tr>
<td>8</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>544.73</td>
<td>317.45</td>
<td>241.63</td>
<td>25.82</td>
<td>0.53e+03</td>
<td>2.1</td>
<td>270.5</td>
<td>104.0</td>
<td>53.3</td>
<td>0.64e+03</td>
<td>0.13e+03</td>
<td>82.5</td>
</tr>
<tr>
<td>9</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>113.42</td>
<td>241.30</td>
<td>230.67</td>
<td>26.57</td>
<td>0.60e+03</td>
<td>7.4</td>
<td>291.6</td>
<td>112.6</td>
<td>57.9</td>
<td>0.71e+03</td>
<td>0.15e+03</td>
<td>82.6</td>
</tr>
<tr>
<td>10</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>216.26</td>
<td>543.74</td>
<td>276.38</td>
<td>29.67</td>
<td>0.66e+03</td>
<td>3.8</td>
<td>311.4</td>
<td>120.5</td>
<td>63.0</td>
<td>0.77e+03</td>
<td>0.17e+03</td>
<td>82.8</td>
</tr>
<tr>
<td>11</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>301.61</td>
<td>581.35</td>
<td>256.60</td>
<td>29.18</td>
<td>0.73e+03</td>
<td>2.5</td>
<td>329.7</td>
<td>127.9</td>
<td>68.0</td>
<td>0.83e+03</td>
<td>0.20e+03</td>
<td>83.0</td>
</tr>
<tr>
<td>12</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>504.89</td>
<td>598.42</td>
<td>239.46</td>
<td>26.87</td>
<td>0.80e+03</td>
<td>2.4</td>
<td>346.7</td>
<td>135.1</td>
<td>73.1</td>
<td>0.89e+03</td>
<td>0.23e+03</td>
<td>83.1</td>
</tr>
<tr>
<td>13</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>656.16</td>
<td>585.56</td>
<td>215.38</td>
<td>29.43</td>
<td>0.80e+03</td>
<td>667.7</td>
<td>360.6</td>
<td>104.8</td>
<td>55.4</td>
<td>0.58e+03</td>
<td>0.68e+03</td>
<td>78.6</td>
</tr>
<tr>
<td>14</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>828.30</td>
<td>508.65</td>
<td>202.63</td>
<td>29.49</td>
<td>0.80e+03</td>
<td>669.6</td>
<td>502.2</td>
<td>196.9</td>
<td>52.9</td>
<td>0.52e+03</td>
<td>0.67e+03</td>
<td>79.3</td>
</tr>
<tr>
<td>15</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>1006.45</td>
<td>591.42</td>
<td>185.80</td>
<td>29.55</td>
<td>0.80e+03</td>
<td>742.0</td>
<td>563.6</td>
<td>112.0</td>
<td>59.6</td>
<td>0.60e+03</td>
<td>0.65e+03</td>
<td>78.6</td>
</tr>
<tr>
<td>16</td>
<td>0.15e+05</td>
<td>0.56e-04</td>
<td>1274.56</td>
<td>654.57</td>
<td>164.76</td>
<td>29.66</td>
<td>0.80e+03</td>
<td>557.4</td>
<td>366.5</td>
<td>112.8</td>
<td>59.8</td>
<td>0.66e+03</td>
<td>0.60e+03</td>
<td>74.8</td>
</tr>
</tbody>
</table>

Model results: Iref=375A, arc load
<table>
<thead>
<tr>
<th>Model</th>
<th>load resistance</th>
<th>AC voltage</th>
<th>Transformer core loss</th>
<th>Transformer copper loss</th>
<th>Transformer total loss</th>
<th>Transformer efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1000Ω</td>
<td>500 V</td>
<td>10 W</td>
<td>20 W</td>
<td>30 W</td>
<td>90%</td>
</tr>
<tr>
<td>2</td>
<td>2000Ω</td>
<td>300 V</td>
<td>15 W</td>
<td>30 W</td>
<td>45 W</td>
<td>80%</td>
</tr>
<tr>
<td>3</td>
<td>500Ω</td>
<td>750 V</td>
<td>25 W</td>
<td>50 W</td>
<td>75 W</td>
<td>70%</td>
</tr>
</tbody>
</table>

Note: The values are approximate and may vary depending on the specific application and environmental conditions.
<table>
<thead>
<tr>
<th>J</th>
<th>1F</th>
<th>1S</th>
<th>ETH</th>
<th>ETH</th>
<th>UCEM</th>
<th>OPV</th>
<th>TR-1S</th>
<th>PS</th>
<th>OPI</th>
<th>TJ</th>
<th>TJD</th>
<th>PTTRAN</th>
<th>PDIODE</th>
<th>EFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>75.76</td>
<td>31.72</td>
<td>42.37</td>
<td>56.62</td>
<td>0.46E-04</td>
<td>29.5</td>
<td>32.1</td>
<td>30.5</td>
<td>23.8</td>
<td>0.31E+02</td>
<td>0.26E+03</td>
<td>82.7</td>
</tr>
<tr>
<td>2</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>95.18</td>
<td>62.32</td>
<td>84.91</td>
<td>71.45</td>
<td>0.13E+03</td>
<td>17.9</td>
<td>61.2</td>
<td>38.8</td>
<td>26.8</td>
<td>0.77E+02</td>
<td>0.54E+03</td>
<td>82.1</td>
</tr>
<tr>
<td>3</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>169.91</td>
<td>90.98</td>
<td>121.34</td>
<td>18.52</td>
<td>0.20E+03</td>
<td>34.1</td>
<td>60.1</td>
<td>69.8</td>
<td>28.5</td>
<td>0.14E+03</td>
<td>0.11E+03</td>
<td>80.3</td>
</tr>
<tr>
<td>4</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>262.75</td>
<td>112.50</td>
<td>155.48</td>
<td>19.32</td>
<td>0.27E+03</td>
<td>30.9</td>
<td>113.0</td>
<td>61.9</td>
<td>30.3</td>
<td>0.20E+03</td>
<td>0.17E+03</td>
<td>80.3</td>
</tr>
<tr>
<td>5</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>354.06</td>
<td>159.00</td>
<td>192.43</td>
<td>20.61</td>
<td>0.33E+03</td>
<td>319.5</td>
<td>140.2</td>
<td>89.4</td>
<td>31.9</td>
<td>0.35E+03</td>
<td>0.12E+03</td>
<td>72.8</td>
</tr>
<tr>
<td>6</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>438.64</td>
<td>188.92</td>
<td>210.05</td>
<td>21.66</td>
<td>0.40E+03</td>
<td>491.6</td>
<td>184.6</td>
<td>112.0</td>
<td>34.6</td>
<td>0.48E+03</td>
<td>0.17E+03</td>
<td>71.2</td>
</tr>
<tr>
<td>7</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>547.62</td>
<td>210.54</td>
<td>225.66</td>
<td>22.41</td>
<td>0.47E+03</td>
<td>685.4</td>
<td>225.6</td>
<td>99.7</td>
<td>40.4</td>
<td>0.52E+03</td>
<td>0.20E+03</td>
<td>81.2</td>
</tr>
<tr>
<td>8</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>337.42</td>
<td>235.68</td>
<td>221.18</td>
<td>22.12</td>
<td>0.53E+03</td>
<td>2.7</td>
<td>203.0</td>
<td>109.2</td>
<td>43.9</td>
<td>0.47E+03</td>
<td>0.01E+03</td>
<td>81.2</td>
</tr>
<tr>
<td>9</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>326.54</td>
<td>243.69</td>
<td>221.56</td>
<td>23.78</td>
<td>0.60E+03</td>
<td>1.1</td>
<td>219.5</td>
<td>117.9</td>
<td>47.7</td>
<td>0.52E+03</td>
<td>0.10E+03</td>
<td>81.4</td>
</tr>
<tr>
<td>10</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>315.76</td>
<td>226.62</td>
<td>229.04</td>
<td>24.41</td>
<td>0.64E+03</td>
<td>0.0</td>
<td>235.0</td>
<td>126.7</td>
<td>50.2</td>
<td>0.57E+03</td>
<td>0.11E+03</td>
<td>81.6</td>
</tr>
<tr>
<td>11</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>323.56</td>
<td>237.18</td>
<td>225.75</td>
<td>25.00</td>
<td>0.72E+03</td>
<td>0.0</td>
<td>250.0</td>
<td>135.4</td>
<td>54.0</td>
<td>0.61E+03</td>
<td>0.13E+03</td>
<td>81.7</td>
</tr>
<tr>
<td>12</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>328.58</td>
<td>289.60</td>
<td>233.75</td>
<td>25.55</td>
<td>0.80E+03</td>
<td>0.0</td>
<td>263.7</td>
<td>142.5</td>
<td>58.1</td>
<td>0.65E+03</td>
<td>0.15E+03</td>
<td>81.8</td>
</tr>
<tr>
<td>13</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>339.33</td>
<td>249.02</td>
<td>232.29</td>
<td>25.93</td>
<td>0.86E+03</td>
<td>171.7</td>
<td>273.3</td>
<td>139.2</td>
<td>81.5</td>
<td>0.63E+03</td>
<td>0.28E+03</td>
<td>74.9</td>
</tr>
<tr>
<td>14</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>379.63</td>
<td>236.12</td>
<td>256.16</td>
<td>26.04</td>
<td>0.93E+03</td>
<td>290.7</td>
<td>276.1</td>
<td>96.7</td>
<td>119.5</td>
<td>0.37E+03</td>
<td>0.36E+03</td>
<td>79.4</td>
</tr>
<tr>
<td>15</td>
<td>0.15E+05</td>
<td>0.45E-04</td>
<td>281.38</td>
<td>449.10</td>
<td>237.10</td>
<td>26.16</td>
<td>0.10E+02</td>
<td>316.2</td>
<td>285.2</td>
<td>93.1</td>
<td>114.6</td>
<td>0.35E+03</td>
<td>0.35E+03</td>
<td>79.5</td>
</tr>
<tr>
<td>16</td>
<td>0.15E+05</td>
<td>0.45E-04</td>
<td>301.32</td>
<td>474.42</td>
<td>228.03</td>
<td>26.24</td>
<td>0.11E+02</td>
<td>301.3</td>
<td>283.8</td>
<td>116.1</td>
<td>113.2</td>
<td>0.41E+03</td>
<td>0.49E+03</td>
<td>79.4</td>
</tr>
<tr>
<td>17</td>
<td>0.15E+05</td>
<td>0.45E-04</td>
<td>412.24</td>
<td>447.54</td>
<td>230.32</td>
<td>26.35</td>
<td>0.11E+02</td>
<td>324.9</td>
<td>283.8</td>
<td>116.1</td>
<td>113.2</td>
<td>0.48E+03</td>
<td>0.46E+03</td>
<td>79.0</td>
</tr>
</tbody>
</table>

Model results @ 300A, arc load
Model results @ 250A, short circuit load

<table>
<thead>
<tr>
<th>J</th>
<th>TR</th>
<th>TKS</th>
<th>TIP</th>
<th>IFP</th>
<th>UCER</th>
<th>OPV</th>
<th>TR-TF</th>
<th>PS</th>
<th>OP1</th>
<th>TJ</th>
<th>TJD</th>
<th>CALA</th>
<th>EFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>85.62</td>
<td>59.50</td>
<td>62.57</td>
<td>1.50</td>
<td>0.60E-04</td>
<td>31.8</td>
<td>55.8</td>
<td>33.6</td>
<td>26.6</td>
<td>0.44E+00</td>
<td>0.27E+01</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>139.96</td>
<td>185.50</td>
<td>136.36</td>
<td>2.82</td>
<td>0.13E+03</td>
<td>46.3</td>
<td>109.0</td>
<td>52.8</td>
<td>50.3</td>
<td>0.15E+03</td>
<td>0.20E+02</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>281.81</td>
<td>291.56</td>
<td>198.24</td>
<td>4.07</td>
<td>0.20E+03</td>
<td>89.7</td>
<td>156.9</td>
<td>82.2</td>
<td>55.9</td>
<td>0.32E+03</td>
<td>0.43E+02</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>286.27</td>
<td>286.37</td>
<td>229.86</td>
<td>5.35</td>
<td>0.27E+03</td>
<td>112.8</td>
<td>206.1</td>
<td>116.1</td>
<td>45.0</td>
<td>0.51E+03</td>
<td>0.85E+02</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>240.64</td>
<td>240.95</td>
<td>222.25</td>
<td>5.35</td>
<td>0.53E+03</td>
<td>231.6</td>
<td>206.1</td>
<td>116.1</td>
<td>45.0</td>
<td>0.51E+03</td>
<td>0.85E+02</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>344.52</td>
<td>344.52</td>
<td>225.34</td>
<td>5.35</td>
<td>0.40E+03</td>
<td>249.0</td>
<td>229.5</td>
<td>74.9</td>
<td>115.0</td>
<td>0.25E+03</td>
<td>0.48E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>356.35</td>
<td>356.35</td>
<td>228.24</td>
<td>5.35</td>
<td>0.47E+03</td>
<td>256.3</td>
<td>244.9</td>
<td>71.2</td>
<td>124.5</td>
<td>0.23E+03</td>
<td>0.55E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>359.79</td>
<td>360.04</td>
<td>229.31</td>
<td>6.05</td>
<td>0.47E+03</td>
<td>260.2</td>
<td>238.2</td>
<td>71.4</td>
<td>133.1</td>
<td>0.23E+03</td>
<td>0.59E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>359.01</td>
<td>359.01</td>
<td>223.07</td>
<td>6.11</td>
<td>0.47E+03</td>
<td>276.8</td>
<td>240.4</td>
<td>71.1</td>
<td>137.0</td>
<td>0.22E+03</td>
<td>0.61E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>359.99</td>
<td>441.41</td>
<td>240.40</td>
<td>6.11</td>
<td>0.47E+03</td>
<td>291.0</td>
<td>241.6</td>
<td>69.8</td>
<td>149.1</td>
<td>0.21E+03</td>
<td>0.63E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>360.42</td>
<td>441.88</td>
<td>241.57</td>
<td>6.17</td>
<td>0.47E+03</td>
<td>294.8</td>
<td>242.8</td>
<td>70.2</td>
<td>141.0</td>
<td>0.22E+03</td>
<td>0.63E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>374.49</td>
<td>474.49</td>
<td>266.82</td>
<td>6.18</td>
<td>0.47E+03</td>
<td>382.1</td>
<td>243.0</td>
<td>70.3</td>
<td>144.6</td>
<td>0.21E+03</td>
<td>0.63E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>378.16</td>
<td>478.20</td>
<td>268.76</td>
<td>6.18</td>
<td>0.47E+03</td>
<td>390.5</td>
<td>243.2</td>
<td>70.8</td>
<td>144.9</td>
<td>0.22E+03</td>
<td>0.65E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>378.96</td>
<td>478.96</td>
<td>269.06</td>
<td>6.18</td>
<td>0.47E+03</td>
<td>391.7</td>
<td>243.4</td>
<td>70.9</td>
<td>145.0</td>
<td>0.22E+03</td>
<td>0.65E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>370.51</td>
<td>477.78</td>
<td>269.25</td>
<td>6.19</td>
<td>0.47E+03</td>
<td>392.4</td>
<td>243.6</td>
<td>70.9</td>
<td>145.1</td>
<td>0.22E+03</td>
<td>0.65E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>370.53</td>
<td>477.76</td>
<td>269.45</td>
<td>6.19</td>
<td>0.47E+03</td>
<td>392.5</td>
<td>243.8</td>
<td>70.9</td>
<td>145.3</td>
<td>0.22E+03</td>
<td>0.65E+03</td>
</tr>
<tr>
<td>0</td>
<td>0.15E+05</td>
<td>0.56E-04</td>
<td>373.26</td>
<td>475.14</td>
<td>269.60</td>
<td>6.20</td>
<td>0.47E+03</td>
<td>393.7</td>
<td>243.9</td>
<td>71.0</td>
<td>145.4</td>
<td>0.22E+03</td>
<td>0.65E+03</td>
</tr>
</tbody>
</table>

Model results @ 250A, short circuit load
### Table: Model Results

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0501</td>
<td>Operating Temperature</td>
<td>85°C</td>
</tr>
<tr>
<td>1.0502</td>
<td>Operating Voltage</td>
<td>450V</td>
</tr>
<tr>
<td>1.0503</td>
<td>AC/DC Power Supply</td>
<td>2.4V</td>
</tr>
<tr>
<td>1.0504</td>
<td>DC/AC Power Supply</td>
<td>4.2V</td>
</tr>
<tr>
<td>1.0505</td>
<td>Input Voltage</td>
<td>4.2V</td>
</tr>
<tr>
<td>1.0506</td>
<td>Output Voltage</td>
<td>4.2V</td>
</tr>
<tr>
<td>1.0507</td>
<td>Input Current</td>
<td>2.4A</td>
</tr>
<tr>
<td>1.0508</td>
<td>Output Current</td>
<td>2.4A</td>
</tr>
<tr>
<td>1.0509</td>
<td>Input Power</td>
<td>5.76W</td>
</tr>
<tr>
<td>1.0510</td>
<td>Output Power</td>
<td>5.76W</td>
</tr>
<tr>
<td>1.0511</td>
<td>Input Efficiency</td>
<td>95.5%</td>
</tr>
<tr>
<td>1.0512</td>
<td>Output Efficiency</td>
<td>95.5%</td>
</tr>
</tbody>
</table>

Note: All values are in units specified by the respective columns.
APPENDIX B

Data sheets for
- MEDL DT63 Transistor
- Thomson CSF ESM3001 Transistor
- MEDL TC40U Transistor
- Westinghouse Electric Fast recovery diode R622
- Thomson CSF Fast recovery diode BYW78 - 200
- Thomson CSF Fast recovery diode ESM243 400
- RIFA metallised polypropylene capacitor
- ICW metallised polypropylene capacitor
- MEDL EDN range of heatsinks
**APPLICATIONS**
- High Frequency Inverters
- Motor Controls
- Switching Regulators
- VLF Transmitters
- Induction Heating
- Power Supplies

**FEATURES**
- Double Sided Cooling Capability
- Triple Diffused
- High Power Capability
- Wide F50A and RB50A
- Thermal Fatigue Free Compression Bonded Structure
- Fast Switching
- Parameters characterised at 125°C

<table>
<thead>
<tr>
<th>RATINGS</th>
<th>CONDITIONS</th>
<th>D163-500</th>
<th>D163-400</th>
<th>D163-300</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCEO(min)Collector-emitter sustaining</td>
<td>IC = 500mA</td>
<td>350</td>
<td>300</td>
<td>250</td>
</tr>
<tr>
<td>VCEO(min)Emitter-base sustaining (i) voltage</td>
<td>IB = 0</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>VCEO(min)Continuous collector current</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>VCEO(max)Collector cut-off current</td>
<td>At rated VCEO</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>VCEO(max)Emitter cut-off current</td>
<td>VCE = -1.5V</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

**OFF-STATE CHARACTERISTICS**

| VCE(sat)Collector-emitter saturation voltage | IC = 200A | 0.6125 | 0.6125 | 0.6125 | V |
| VCE(sat)Emitter-base saturation voltage | IB = (IC/hfe)1.5 | 1.2 | 1.75 | 1.2 | 1.75 | V |
| hFE | DC current gain | IC = 200A | 11 | 12 | 13 |

(1) NOTE: VCEO(SUS) and VCEO(SUS) must not be measured on a curve tracer.
**DT63 SERIES**

\[ V_{CE\text{(SUS)}} = 400/350/300 \text{ V} \]
\[ V_{CEX} = 500/400/300 \text{ V} \]
\[ I_C\text{(CONT)} = 400 \text{ A} \]
\[ I_C\text{(MAX)} = 450 \text{ A} \]
\[ t_F(125^\circ C) = 0.8 \mu s \]

**'POWERLINE'**

**NPN TRANSISTOR RANGE**

---

**TEST CONDITIONS**

**Switching Characteristics** Clamped inductive load \( T_C = 125^\circ C \)

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>DT63-500</th>
<th>DT63-400</th>
<th>DT63-300</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage time ( t_s )</td>
<td>( V_{CE\text{(SUS)}} ) 3.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Fall time ( t_F )</td>
<td>( I_C ) 0.8</td>
<td>0.8</td>
<td>0.8</td>
</tr>
</tbody>
</table>

---

**DC Current Gain \( h_{fe} \)**

<table>
<thead>
<tr>
<th>Collector Current ( I_C ) (Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

**Collector Current \( I_C \) (Amps)**

TYPICAL DC FORWARD CURRENT TRANSFER RATIO

![Graph showing DC Current Gain](image)

---

**Typical Saturation Voltage**

<table>
<thead>
<tr>
<th>Collector Current ( I_C ) (Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>0.2</td>
</tr>
<tr>
<td>0.4</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>0.8</td>
</tr>
<tr>
<td>1.0</td>
</tr>
</tbody>
</table>

TYPICAL SATURATION VOLTAGE

![Graph showing Saturation Voltage](image)
**DT63 SERIES**

**VCE(SUS)** = 400/350/300 V  
**VCEX** = 500/400/300 V  
**IC(CONT)** = 400 A  
**IC(PK)** = 450 A  
**t_f (125°C)** = 0.8 μs

---

**TYPICAL VBE versus COLLECTOR CURRENT CHARACTERISTICS**

1. Emitter-Base diode maintains reverse bias across Emitter-Base during off-state and clamps Emitter-Base junction during clamped inductive load turn-off.
2. Load line tailoring required when switching at peak current.
### Tentative Data

**SUPERSWITCH**

**HIGH CURRENT, HIGH POWER TRANSISTOR**

Pressure contact construction  
Thermal fatigue free

- * High current capability
- Very low saturation resistance at 100 °C
- High specified gain at 100 A
- Fast turn-on and turn-off

### Absolute Ratings (Limiting Values)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ESM 3000</th>
<th>ESM 3001</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCEOout</td>
<td>100 V</td>
<td>150 V</td>
</tr>
<tr>
<td>VCEX</td>
<td>200 V</td>
<td>200 V</td>
</tr>
<tr>
<td>I_Csat</td>
<td>150 A</td>
<td>150 A</td>
</tr>
<tr>
<td>I_CM</td>
<td>300 A</td>
<td>300 A</td>
</tr>
<tr>
<td>R(ON)sat</td>
<td>&lt; 7 mΩ</td>
<td>@ 100 °C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Collector-emitter voltage</th>
<th>VCEO</th>
<th>100 V</th>
<th>150 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter voltage</td>
<td>VCEX</td>
<td>200 V</td>
<td>200 V</td>
</tr>
<tr>
<td>Emitter-base voltage</td>
<td>V_EBD</td>
<td>7 V</td>
<td>7 V</td>
</tr>
<tr>
<td>Collector current</td>
<td>I_CM</td>
<td>300 A</td>
<td>300 A</td>
</tr>
<tr>
<td>Base current</td>
<td>I_B</td>
<td>20 A</td>
<td>20 A</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>P_Dot</td>
<td>400 W</td>
<td>400 W</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>T_J</td>
<td>-65 + 175 °C</td>
<td></td>
</tr>
</tbody>
</table>

**Junction-case thermal resistance**  
Resistivité thermique jonction-boîtier

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ESM 3000-3001</th>
<th>ESM 4000-4001</th>
</tr>
</thead>
<tbody>
<tr>
<td>R(θj-cl)</td>
<td>0.25</td>
<td>0.25</td>
</tr>
<tr>
<td>Double sided cooling</td>
<td>0.13</td>
<td>0.13</td>
</tr>
</tbody>
</table>

* September 1981 1/2*
### ELECTRICAL CHARACTERISTICS - CARACTÉRISTIQUES ÉLECTRIQUES **

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>UNITS</th>
<th>TEST CONDITIONS - CONDITIONS DE MESURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEO\text{on}}$</td>
<td>100</td>
<td>150</td>
<td>V</td>
<td>ESM 3000-4000 ESM 3001-4001</td>
<td>8 = 0, L = 25 mH, $I_C = 0.5$ A</td>
</tr>
<tr>
<td>$V_{IBRIEDO}$</td>
<td>7</td>
<td>V</td>
<td>$I_C = 5$, $I_g = 100$ mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CEX}$</td>
<td>6</td>
<td>mA</td>
<td>$V_{CE} = 200$ V, $V_{BE} = -1.5$ V, $T_J = 126$ °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CE}$</td>
<td>10</td>
<td>mA</td>
<td>$V_{CE} = 200$ V, $R_{BE} = 10$ Ω, $T_J = 126$ °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{EBO}$</td>
<td>30</td>
<td>mA</td>
<td>$I_C = 0$, $V_{EB} = 5$ V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### OFF CHARACTERISTICS - CARACTÉRISTIQUES À L’ÉTAT BLOQUÉ

| $V_{CE\text{sat}}$ | 1.5 | V | $I_C = I_{C\text{sat}} = 150$ A, $I_g = I_{B\text{sat}} = 15$ A |
| 1.5 | |
| 0.7 | |
| 0.5 | |
| $V_{BE\text{sat}}$ | 1.7 | V | $I_C = I_{C\text{sat}}$, $I_g = I_{B\text{sat}}$, $T_J = 100$ °C |

### ON CHARACTERISTICS - CARACTÉRISTIQUES À L’ÉTAT CONDUCTEUR

| $V_{CC}$ | 60 V, $I_C = I_{C\text{sat}}$ (1) | $T_J = 100$ °C |
| $I_{B1} = -I_{B2} = I_{B\text{sat}}$ |

### SWITCHING CHARACTERISTICS - CARACTÉRISTIQUES DE COMMUTATION

#### Resistive load - Charge résistive

| $t_{on}$ | 1.5 | μs |
| $t_q$ | 1.8 | μs |
| $t_f$ | 0.6 | μs |

#### Inductive load - Charge inductif

| $t_f$ | 0.3 | μs |
| $t_f$ | 0.5 | μs |

*Measured with pulses $t_D = 300$ μs $\leq 2$ % ** $T_{CASE} 25$ °C Unless otherwise stated (1) $V_{CE}\text{clamp} < V_{CE\text{on}}$

---

**Important Notes and References:**

- Case outline CB 183
- Case outline MU 86 (CB 262)
FIGURE 1: DC and AC pulse area.

FIGURE 2: Collector-emitter voltage vs base-emitter resistance.

FIGURE 3: Power and \( I_{PB} \) derating vs case temperature.

FIGURE 4: Transient thermal response.

FIGURE 5: Case outline - TO 83 (CB 183)
SWITCHING OPERATING AND OVERLOAD AREAS

TRANSISTOR FORWARD BIASED
- During the turn on
- During the turn off without negative base-emitter voltage and $R_{BE} \geq 3 \Omega$

![Forward biased safe operating area (FBSOA)](image)

LIMITS
- Limit only for turn on and turn off
- Limit for turn on

FIGURE 12: Forward biased safe operating area (FBSOA)

TRANSISTOR REVERSE BIASED
- During the turn off with negative base-emitter voltage

![Reverse biased safe operating area (RBSSOA)](image)

FIGURE 13: Reverse biased safe operating area (RBSSOA)

LIMITS
- Limit only for turn on and turn off
- Limit for turn on

FIGURE 14: Forward biased accidental overload area (FBAOA)

FIGURE 15: Reverse biased accidental overload area (RBAOA)

Figure 12: The hatched zone can only be used for turn on.

Figures 14 and 15: High accidental surge currents ($I > I_{CM}$) are allowed if they are non-repetitive and applied less than 3000 times during the component life.

Figure 14: The Kellog network (heavy print) allows the calculation of the maximum value of the short-circuit current for a given base current $I_{B}$ ($90 \%$ confidence).

Figure 15: After the accidental overload current, the RBADA has to be used for the turn off.
RESISTIVE LOAD

\[ I_c = \frac{10}{I_B} \]

\[ V_C = 90 \, V \]

FIGURE 16: Switching times vs collector current (resistive load)

INDUCTIVE LOAD

\[ V_{CC} = 90 \, V \]

\[ I_c = 10 \, \mu A \]

FIGURE 17: Switching times vs collector current

FIGURE 18: Switching times vs junction temperature
**APPLICATIONS**
- Switching Regulators
- Motor Drive Controls
- High Power Switching Currents

**FEATURES**
- Double Diffused Planar Epitaxial Structure
- 'HIVOX' Passivated
- Low Vc(eSat)
- Extremely Fast Switching
- Single Chip Construction

**TC40U SERIES**
- \( I_{C(\text{CONT})} = 40\,\text{A} \)
- \( I_{C(\text{PK})} = 70\,\text{A} \)
- \( V_{CEX(SUS)} = 150/200/286\,\text{V} \)
- \( t_f < 0.5\,\text{pS} \)

**APPLICATIONS**
- Switching Regulators
- Motor Drive Controls
- High Power Switching Currents

**FEATURES**
- Double Diffused Planar Epitaxial Structure
- 'HIVOX' Passivated
- Low Vc(eSat)
- Extremely Fast Switching
- Single Chip Construction

---

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>TC40U - 150</th>
<th>TC40U - 250</th>
<th>TC40U - 300</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CEX(SUS)} )</td>
<td>Collector-emitter sustaining voltage</td>
<td>100</td>
<td>150</td>
<td>250</td>
</tr>
<tr>
<td>( V_{CEX} )</td>
<td>Collector-emitter voltage</td>
<td>( V_{BE} = -1.5,\text{V} )</td>
<td>200</td>
<td>250</td>
</tr>
<tr>
<td>( I_{C(\text{CONT})} )</td>
<td>Continuous collector current</td>
<td>40</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>( I_{C(\text{PK})} )</td>
<td>Peak collector current</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>( I_{EBO} )</td>
<td>Collector cut-off current</td>
<td>70</td>
<td>79</td>
<td>70</td>
</tr>
<tr>
<td>( P_{TOT} )</td>
<td>Power dissipation</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>( T_j )</td>
<td>Junction Temperature</td>
<td>175</td>
<td>175</td>
<td>175</td>
</tr>
<tr>
<td>( V_{CEX} )</td>
<td>Collector-emitter voltage</td>
<td>( V_{BE} = -1.5,\text{V} )</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>( I_{EBO} )</td>
<td>Emitter cut-off current</td>
<td>At rated ( V_{CEX} )</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>( R_{j-C} )</td>
<td>Thermal resistance (junction to heatsink)</td>
<td>0.85</td>
<td>0.85</td>
<td>0.85</td>
</tr>
<tr>
<td>( h_{FE} )</td>
<td>DC Current Gain</td>
<td>( I_C = 20A; V_{CE} = 10V )</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>( h_{	ext{fmax}} )</td>
<td>Fall time</td>
<td>( I_C = 20A; V_{CC} = 200,\text{V} )</td>
<td>2.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

---

**SYMBOL TEST CONDITIONS**

**ABSOLUTE MAXIMUM RATINGS** (at \( T_c = 25\,\text{°C} \) unless specified)

- \( V_{CEX(SUS)} \) (max)
- \( I_{EBO} \) (max)
- \( I_{CEX} \) (max)
- \( R_{j-C} \) (J-C)
- \( h_{FE} \) (max)
- \( h_{fmax} \) (max)
- \( T_{4} \) (max)
- \( T_{f} \) (max)

---

**OFF-STATE CHARACTERISTICS** (at \( T_c = 25\,\text{°C} \) unless specified)

- \( V_{CEX(SUS)} \) (max)
- \( I_{C(\text{CONT})} \) (max)
- \( I_{EBO} \) (max)
- \( R_{j-C} \) (J-C)

---

**ON-STATE CHARACTERISTICS** (at \( T_c = 25\,\text{°C} \)

- \( V_{CEX(SUS)} \) (max)
- \( I_{C(\text{CONT})} \) (max)
- \( I_{EBO} \) (max)
- \( R_{j-C} \) (J-C)

---

**SWITCHING CHARACTERISTICS — Resistive**

(See Appendix II)

- \( I_{C} \) (max)
- \( \mu S \)
- \( T_{C} \) (max)
- \( V_{CC} \) (200V)
- \( I_{B} \) (2A)
- \( I_{E} \) (2A)
- \( V_{CEX} \) (286V)
- \( T_{f} \) (max)
- \( \mu S \)

---

**Issue 1 Dec. 1981**

Marconi Electronic Devices Limited
Carholme Road, Lincoln LN1 1SG England
Telephone (0522) 29992 Telex 56163
MEDL ‘POWERLINE’
NPN TRANSISTOR RANGE

TC40U SERIES
Ic(CONT) = 40A
Ic(PK) = 70A
VCEO(SUS) = 150/200/286V
tf ≤ 0.5μs

DISSIPATION AND Ic/B DERATING

SAFE OPERATING AREA

Typical Static Forward Current Transfer Ratio
TC40U SERIES

$V_{CEX(SUS)} = 150/200/286V$

$t_f < 0.5\mu s$

**TYPICAL SATURATION VOLTAGE**

- $V_{CE} = 1.0\text{ SATURATION VOLTS}$
- $T_c = 150^\circ C$
- $T_c = 65^\circ C$
- $T_c = 25^\circ C$
- $I_C = 5$
- $I_B$

**TYPICAL SWITCHING TIME**

- $V_{CC} = 200V$
- $I_B1 = 2A$
- $I_B2 = 4A$
- $T_j = 25^\circ C$

**COLLECTOR CURRENT $I_C$ (A)**
Soft-Fast Recovery
RECTIFIER
R622 ... 30
300 A. Avg.
Up to 1200 Volts
500 ns

Symbol | Inches | Millimeters
---|---|---
ØD | 1.610 - 1.650 | 40.85 - 41.91
ØD₂ | 745 - 755 | 18.92 - 18.18
ØD₃ | 1.420 - 1.460 | 36.07 - 37.08
H | 5.00 - 5.60 | 12.70 - 14.22
ØJ | 1.36 - 1.45 | 3.43 - 3.68
Ω | 0.72 - 0.82 | 1.83 - 2.08
N | 0.30 - 0.76 |

Creep Distance—48 in. min. (12.60 mm).
Stress Distance—82 in. min. (21.27 mm).
(1 in. = 25.4 m m).
Finish—Nickel Plate.
Approx Weight—2.3 oz (66 g).

Ordering Information

<table>
<thead>
<tr>
<th>Type</th>
<th>Voltage Code</th>
<th>Current I (A)</th>
<th>Recovery Time n sec</th>
<th>Leads</th>
</tr>
</thead>
<tbody>
<tr>
<td>R622</td>
<td>400 04</td>
<td>3.00</td>
<td>300</td>
<td>PS R62 00</td>
</tr>
<tr>
<td></td>
<td>600 06</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>700 07</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>800 08</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>900 09</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1000 10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1100 11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1200 12</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example

Obtain optimum device performance for your application by selecting proper Order Code.
Type R622 rated at 300A average with Vrms = 1200V, and 500 nsec recovery time order as:

Westinghouse Electric Corporation • Semiconductor Division • Youngwood, Pa. 15697
300 A. Avg.  
Up to 1200 Volts  
500 ns  

**Voltage**  
Blocking State Maximums  
Symbol

- Repetitive peak reverse voltage, V\(_{\text{VFM}}\)  
- Non-repetitive transient peak reverse voltage, V\(_{\text{VFM}}\)  
- Reverse leakage current, mA peak  

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td></td>
</tr>
<tr>
<td>800</td>
<td></td>
</tr>
<tr>
<td>700</td>
<td></td>
</tr>
<tr>
<td>900</td>
<td></td>
</tr>
<tr>
<td>800</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>900</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>1200</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>1300</td>
<td></td>
</tr>
<tr>
<td>1400</td>
<td></td>
</tr>
</tbody>
</table>

**Current**  
Conducting State Maximums  
 Symbol

- RMS forward current, A\(_{\text{If}}\)  
- Ave. forward current, A\(_{\text{If}}\)  
- One-half cycle surge current, A\(_{\text{If}}\)  
- 10 cycle surge current, A\(_{\text{If}}\)  
- Forward voltage drop at I\(_{\text{If}}\) = 800 A and T\(_J\) = 25\(^\circ\)C, V\(_{\text{VFM}}\)  

<table>
<thead>
<tr>
<th>Current</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>470</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td></td>
</tr>
<tr>
<td>3600</td>
<td></td>
</tr>
<tr>
<td>2700</td>
<td></td>
</tr>
<tr>
<td>2100</td>
<td></td>
</tr>
<tr>
<td>51,000</td>
<td></td>
</tr>
</tbody>
</table>

**Switching**  
(T\(_J\) = 25\(^\circ\)C)  
Symbol

- Max. Reverse Recovery Characteristics  
- Max. Reverse Recov. Current, I\(_{\text{rrm}}\)  
- di/dt  
- T\(_C\) = 150\(^\circ\)C  

<table>
<thead>
<tr>
<th>Switching</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 mA</td>
<td></td>
</tr>
<tr>
<td>7.5 A</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>1.1 (\mu)s</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal and Mechanical**  
Symbol

- Min. Max. oper. junction temp., \(\degree\)C  
- Min. Max. storage temp., \(\degree\)C  
- Max. mounting torque, in lb  
- Junction to case, \(\degree\)C/Watt  
- Case to sink, lubricated \(\degree\)C/Watt  

<table>
<thead>
<tr>
<th>Thermal and Mechanical</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40 to +150</td>
<td></td>
</tr>
<tr>
<td>-40 to +190</td>
<td></td>
</tr>
<tr>
<td>1000 to 1400</td>
<td></td>
</tr>
<tr>
<td>0.95</td>
<td></td>
</tr>
<tr>
<td>0.025</td>
<td></td>
</tr>
</tbody>
</table>
**FAST RECOVERY SUPERSWITCH RECTIFIERS**

- **VERY FAST RECOVERY TIME**
- **VERY LOW RECOVERED CHARGE**
- **VERYL LOW FORWARD RECOVERY TIME**

**APPLICATIONS**
- High frequency choppers
- DC and AC motor control
- Switchmode power supply

**APPLICATIONS**
- Hauteurs à fréquence élevée
- Commandes de moteurs continus et alternatifs
- Alimentation à découpage

---

**ABSOLUTE RATINGS (LIMITING VALUES)**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>ESM 243 50</th>
<th>ESM 243 100</th>
<th>ESM 243 200</th>
<th>ESM 243 300</th>
<th>ESM 243 400</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC reverse voltage</td>
<td>$V_R$</td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>Peak reverse voltage</td>
<td>$V_{RRM}$</td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>Repetitive peak reverse voltage</td>
<td>$V_{RRM}$</td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>Average forward current (1) $T_{case} 90^\circ C$</td>
<td>$I_{F(AV)}$</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>Peak one cycle surge current (sinusoidal tp 10 ms)</td>
<td>$I_{FSM}$</td>
<td>800</td>
<td>3200</td>
<td>800</td>
<td>3200</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>$T_{(j)}$</td>
<td>-65 +165</td>
<td>-65 +165</td>
<td>-65 +165</td>
<td>-65 +165</td>
</tr>
</tbody>
</table>

**Junction-case thermal resistance max**

$R_{ph(l-j)}$ max | 0.7 | 0.7 | 0.7 | 0.7 | 0.7 | °C/W

---

1. See figure 3.
2. Voir figure 3.

Janvier 1982 1/7
HIGH EFFICIENCY SUPERSWITCH

LOW VOLTAGE DROP RECTIFIERS SUITED FOR SWITCHMODE POWER SUPPLY.

- Very low conduction losses
- Negligible switching losses
- Low forward and reverse recovery times
- High surge current and avalanche capability
- The specifications and curves enable the determination of \( t_{rr} \) and \( I_{RM} \) at 100 °C under users conditions.
- Ease of paralleling

REDRESSEURS A FAIBLE CHUTE DE TENSION ADAPTES AUX ALIMENTATIONS A DECOUPAGE

- Très faibles pertes de conductance
- Péres de commutation négligeables
- Faibles temps de recouvrement inverse et direct
- Courant de surcharge et d'avalanche élevé
- Les caractéristiques et les courbes permettent de déterminer \( t_{rr} \) et \( I_{RM} \) à 100 °C dans les conditions d'utilisation
- montage en parallèle facile

<table>
<thead>
<tr>
<th>Absolute Ratings (Limiting Values)</th>
<th>BYW 78-50</th>
<th>BYW 78-100</th>
<th>BYW 78-150</th>
<th>BYW 78-200</th>
<th>BYW 78-150 A avalanche</th>
</tr>
</thead>
<tbody>
<tr>
<td>Repetitive peak reverse voltage ( V_{RRM} )</td>
<td>50</td>
<td>100</td>
<td>150</td>
<td>200</td>
<td>150</td>
</tr>
<tr>
<td>Repetitive peak reverse voltage ( V_{RSM} )</td>
<td>55</td>
<td>110</td>
<td>165</td>
<td>220</td>
<td>—</td>
</tr>
<tr>
<td>Peak surge non-repetitive reverse power dissipation ( P_{(1)} )</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2,3 kW</td>
<td></td>
</tr>
<tr>
<td>Power dissipation ( P )</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
</tr>
</tbody>
</table>

\( V_F \) < 0.85 V @ 50 A
\( V_{RRM} \) 50 → 200 V
\( I_{(1)AV} \) 50 A @ \( T_c \) 100 °C
\( t_{rr} \) < 60 ns
\( P_{RSM} \) 2,3 KW

Case Boîtier DO 5 (CB 34)

ISO M6 : BYW 78-50 M → BYW 78-200 M
1/4-28 UNF : BYW 78-50 → BYW 78-200

(1) BYW 78-150 A \( t_p = 80 \mu s \) - sinusoidal | Controlled avalanche type

Junction case thermal resistance \( R_{th(j-c)} \) : 1 1 1 1 1 RC. IV
Commutating and Snubber Protection Capacitors

PHU 482-483 is a range of metallized polypropylene capacitors specially designed for low losses and low series resistance. Other characteristics are high pulse current capability and small dimensions. The metallized polypropylene construction is characterized by self-healing in the event of dielectric breakdown without any interruption of operation. High voltage of short duration will not therefore damage the capacitor, and the series provides excellent performance in conditions where high pulse voltages and high transients occur.

Special characteristics

- High charging and discharging current capability
- High insulation resistance
- Low losses
- Low impedance
- Good stability
- Excellent self-healing properties

Applications

Primarily as commutating capacitors or protection capacitors in combination with a resistance in thyristor circuits. The capacitors are also suitable for all non-sine wave applications.

Rated Voltage

- Rated Voltage: 750 V 50–60 Hz
- Peak Voltage: 1000 V
- Temperature Range: -40°C to +85°C
- Climatic Category: DIN GPF, IEC 40/085/56
- Life Expectancy: The capacitors are designed for a life expectancy of 30,000 hours with an estimated survival of 95% when operated at rated voltage and at rated case temperature.

Construction

Metallized polypropylene capacitor element with sprayed metallized ends to which the termination leads are welded, thus ensuring low self-inductance and reliable contact even at low working voltages. The element is assembled in a vibration-proof way in a tubular aluminium can, which is hermetically sealed by epoxy resin. Terminations at one end. Fixing is provided by the centre bolt.

Mechanical Solidity

IEC 68-2-29, test Eb. The capacitors will withstand at least 4000 bumps with 390 m/s² retardation in any position, when mounted in a secure manner.

Terminals

Flexible 2.5 mm² tinned copper leads of 250 mm length.

Mounting

The capacitors can be mounted in any position.

Marking

The capacitors are marked with capacitance, capacitance tolerance, rated voltage, temperature range, article No., date of manufacture in code, climatic category according to DIN and RIFA symbol.
General Specification

These devices are designed to operate at very high values of Peak and RMS Current. They are supplied un-housed, with no conventional terminals and are intended to be clamped between two conductive surfaces, possibly heat sinks. This assembly ensures that heat generated within the device is conducted away most efficiently, allowing the maximum amount of power to be dissipated whilst maintaining a satisfactory temperature increase. The range has been developed to meet the very exacting conditions encountered in modern Thyristor Motor Speed Controllers which employ fast turn-off Thyristors and require high current Capacitors packaged in the smallest possible volume. The dielectric material is polyester but other materials can be supplied if required.

Electrical Characteristics

Capacitance Tolerance:
±10% Standard, others on request

Insulation Resistance:
> 10,000 Ohm-Farad (seconds) measured at working voltage and 20±5°C

Dissipation Factor:
< 0.008 — Polyester
   Measured at 1KHz and 20±5°C

Proof Voltage Test:
1.5x Working Voltage for 30s not to be repeated

Peak / RMS Currents:
Dependent on several factors, including Working Voltage, Voltage Waveform and "Aspect Ratio"
Dielectric constant $\varepsilon$ of Hostaphan RE 6 µm (25 gge) in the temperature range of $-60$ to $160^\circ$ C, determined at a frequency of 50 Hz.

Dissipation factor tan $\delta$ of Hostaphan RE 6 µm (25 gge) in the frequency range of $10^1$ — $10^4$ Hz at $-50^\circ$ C, $20^\circ$ C and $150^\circ$ C.

Technical data for Hostaphan RS

<table>
<thead>
<tr>
<th>Property</th>
<th>Approximate value</th>
<th>Unit</th>
<th>Test standard specification</th>
<th>Test conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>1.39</td>
<td>g/cm$^3$</td>
<td>ASTM-D 1505-67 method C</td>
<td>$23^\circ$ C</td>
</tr>
<tr>
<td>Tensile strength</td>
<td>$&gt; 120$</td>
<td>N/mm$^2$</td>
<td>DIN 53455 or ASTM D 882-64 T</td>
<td>100% min, 23$^\circ$ C/50% R.H.</td>
</tr>
<tr>
<td>Elongation</td>
<td>$&gt; 80$</td>
<td>%</td>
<td>DIN 53455 or ASTM D 882-64 T</td>
<td>100% min, 23$^\circ$ C/50% R.H.</td>
</tr>
<tr>
<td>Dielectric strength</td>
<td>380 - 9600</td>
<td>kV/mm volts/mil</td>
<td>DIN 40634</td>
<td>23$^\circ$ C/50 Hz</td>
</tr>
<tr>
<td>Dielectric constant ($\varepsilon$)</td>
<td>3.3</td>
<td>--</td>
<td>DIN 40634 or ASTM D 150-65 T</td>
<td>23$^\circ$ C/50 Hz</td>
</tr>
<tr>
<td>Dissipation factor (tan $\delta$)</td>
<td>0.0020</td>
<td>--</td>
<td>DIN 40634 or ASTM D 150-65 T</td>
<td>23$^\circ$ C/50 Hz</td>
</tr>
<tr>
<td>Shrinkage</td>
<td>machine direction</td>
<td>30%</td>
<td>DIN 40634</td>
<td>150$^\circ$ C, 15 min.</td>
</tr>
<tr>
<td></td>
<td>transverse direction</td>
<td>6%</td>
<td>Din 40634</td>
<td></td>
</tr>
</tbody>
</table>

Our range includes the thicknesses 8, 12, 19 and 30 µm in widths of 6 mm and upwards, like Hostaphan RE.
Removal of all burrs.

Material: Aluminium Alloy Extrusion to Directive 1/2/491/A2

Finish: Natural - No Suek Letter to Specification

Notes:
1. Length 'X': 3 standard
   Lengths are:
   - 150 mm: ED 150
   - 225 mm: ED 225
   - 200 mm: ED 200

2. Weight:
   - ED 150: 2.16 kg
   - ED 225: 3.23 kg
   - ED 200: 4.42 kg

Remove all burrs.

Product Code: M3447

Table:

<table>
<thead>
<tr>
<th>Material</th>
<th>Description</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>All products in目录</td>
<td>Devices Limited</td>
<td>MIMAGI ELECTRICAL DEVICES LIMITED</td>
</tr>
<tr>
<td>Unless otherwise stated</td>
<td></td>
<td>LINCOLN</td>
</tr>
<tr>
<td>The following tolerances apply to all dimensions</td>
<td></td>
<td>WEATHERFEATHER LTD</td>
</tr>
<tr>
<td>Up to 200 2504 above</td>
<td></td>
<td>ANKIN</td>
</tr>
<tr>
<td>200 10 559 2510 above</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
VAiation of Thermal resistance with length for ED heating. Force cooled.
**APPENDIX C**

Additional information on welding tests

- Pulsed Current Transfer welding
- Dip Transfer welding
Results obtained for the wire burnoff and droplet detachment experiments

wire burnoff (I=k.W)

Droplet detachment (I_p^2.3, T_p=K)

Influence of mean current on burn off rate (manual welding, 1.2 mm wire)

Detachment phenomena. Wire dia. 1.2 mm.
Macro section of a weld using the chopper power source compared against that from a conventional power source.

Conditions:
- Wire: 1.2mm LW1
- Gas: Argoshield 5

Material: CMn 10mm thickness
Position: Fillet weld in horizontal
Magnification: X 5

Chopper power source

Material: CMn 10mm thickness
Position: Fillet weld in horizontal
Magnification: X 5

Conventional pulse Mig power source

10mm

Vertical section of parent material
Weld joint
Weld penetration points

Horizontal section of parent material
Fusion and reinforcement area variation with arc current

Fusion area

Reinforcement area

Arc current - Amperes

Area - millimetres$^2$
APPENDIX D

Comparable MIG welding power source literature

- GEC M500 Series Linear Regulator
- NEI (Mitsubishi) 2kHz transistor chopper
- AWP M450 15kHz transistor chopper (thesis subject)
- Kemppi PS5000 5kHz thyristor primary inverter
- Fronius Transarc 20kHz transistor primary inverter
With the unique synergic system matching pulse parameters automatically to the wire feed speed, precise MIG welding on the shop floor is available either for mechanised systems or for welder manipulated operation. The M500 provides the following features:

- Stability of output against mains voltage variation of ±15% available.
- Stability against temperature changes.
- Current reproducability between sources of better than 1% at maximum output.
- Current discrimination of 1 Amp.
- Output characteristic variable between constant current and constant voltage.

Instantaneous reactions to demands by the arc provide optimum process stability and weld quality.

SYNERGIC MIG for continuous control of metal transfer.

Programmed conditions for DIP Transfer, Spray and Pulsed current MIG Welding.

The unique synergic system offers the following advantages:

- Stabilised and reproducible welding parameters to high accuracies.
- Accurate wire feed speed control with feedback to the power source.
- Four separate programmes can be stored in the power source and recalled by push-button selection.
- Improved mechanical properties.
- Reduced repair rates.
- More tolerance in welding procedures.
- Less time spent in setting conditions.
- Less operator training for this simplified welding process.
- Ideal for automatic welding applications.
- Variable arc conditions can be obtained for a given mean current and deposition rate.
- Spray transfer mode obtained at arc powers which are considerably lower than in true spray conditions.
- Positional welding achieved without problems of lack of fusion, excessive spatter or poor profile.
Weldcontrol

Nuclear Systems Ltd

Almost spatter-free multi-positional welding of carbon and stainless steel
- Single dial control
- Choice of
  - Clean Mag 200
  - Clean Mag 350
  - Clean Mag 500

2kHz secondary transistor chopper power source
What does the AWP M450 power source do?

- Current levels continuously variable within the range 65 amps to 450 amps.
- A single simplified control provides precise pulsed current output and synchronised wire feed speed at any setting.
- Pulse current frequency and wire feed speed locked together to work in synergic harmony.
- Automatic energy control. The combination of constant current power source output and arc voltage control gives automatic control of the arc energy.
- Automatic wire stick out compensation, equates to constant arc length through constant current.
- The highly important welding parameter, current, is accurately maintained giving optimum control of weld penetration.
- High level of accuracy and repeatability.
- 100% duty cycle at 350 amps and 450 amps at 60%.
- Digital current display.

It comes in two variants to provide you with the following features:

M450S Synergic Power Source
- Pre-set Current pulsed for carbon steel wires in Argon based gases.
- Additional facility as an optional extra — Separate parameter cards for any other metal or alloy i.e. Aluminium, Stainless Steel, etc.
- 3 position wire size selection switch for 1.0mm, 1.2mm and 1.6mm diameter wires.

M450PS Programmable Synergic Power Source
- Facility to set any pulse condition up to 450 amps. This allows any pulsed welding parameters to be set to weld any material.
- Any pulse condition can be programmed into the single control system and varied synergically.

16kHz transistor chopper power source (this thesis)
**What is Synergic MIG?**

With conventional MIG/MAG power sources for pulsed MIG welding, currents are switched between background (pre-heat) and peak (transfer) levels, synchronised to mains input. Arc control is consequently restricted to the output voltage and wire feed speed.

The M450 power source precisely superimposes a strong pulse of high current on the low background current. This pulse melts and detaches one droplet then propels it directly into the weld pool. The wire does not dip into the weld pool, as the molten droplet is only transferred during the high pulse. This results in stable, all positional welding conditions for all metals and alloys.

These pulses are accurately synchronised with the wire feed speed and this combination is called “Synergic Control.” Therefore, using Transistor Control of the M450 power source to give precise setting of pulse parameters to high accuracy and Synergic Control allows easy setting. This results in high performance, simple to use Synergic MIG Welding.

Now the M450 provides an acceptable attractive alternative for fabricators using the TIG method, particularly those concerned in the welding of non-ferrous metals and thin sections.

**Why AWP Synergic MIG?**

Obviously for the following reasons:

- Precise Pulse Control of any level of Peak Current ($I_p$) Background Current ($I_b$) Peak Time ($T_p$) Background Time ($T_b$).
- Optimum welding parameters for any weldable material composition, in any position without the need to compromise.
- Precise repetitability of welding conditions better than 1%, with combined accuracy of ±1% FSD.
- Improved weld quality in all positions with perfect fusion and penetration.
- Elimination of spatter and reduced fume levels.
- Welding with a controlled constant heat input, which improves the mechanical properties.
- Improved productivity since the synergic facility enables use of larger diameter wires in *All Positions* which was not possible hitherto.

**Usable Synergic Range.**

- 0.8mm Diameter @ 85 A — 220A
- 1.2mm Diameter @ 50 A — 200A
- 1.6mm Diameter @ 100 A — 300A
- Freedom from slag entrapment or cold lapping weld defects, to meet stringent quality control procedures on the 'shop floor'.
- Precise pulses in comparison to other commercially available pulse power sources, see diagram below for pulse response with low current application.
- A truly British designed and manufactured welding package for the most demanding fabricator.

[Diagram showing pulse response and ranges]
5kHz primary inverter power source

KEMPPI MULTISYSTEM
SYNERGIC PULSE-MIG.
One machine for synergic MIG, TIG and Manual Metal Arc welding of any metal or alloy from a single power source is revolutionary by any yardstick, and yet that is exactly what the TPS Transarc 500 can do.

Built on the modular system it gives a fabricator facilities basic to his current and future needs with the option of unlimited extension into more sophisticated fields.

This versatility is obtained through the use of "peripherals" — plug in control units which, operating remotely in conjunction with the machine's power source enable a fabricator to pre-select, programme and feed in any required procedure or set of parameters for a given welding job.

**FEATURES AND APPLICATIONS**

- **ROBOT INTERFACE** By stepless control pulsed or non-pulsed, 0-10V DC command from Robot. Synergic, or non-synergic.
- **TIG** Hot, standard or latched start. Variable slope, pulsed or timed sequence. Foot or torch-controlled.
- **PULSED ARC** Synergic programme sixty-three possibilities. Pre-set or hot start with crater fill.
- **MATERIALS** All types of mild and low-carbon steels, stainless steels and aluminium (hot start available); special materials including hard facing applications.
- **DEPOSITION RATE** Increased by up to 30% compared with normal CO₂ welding.
- **WIRE FEEDERS** Static, mobile or boom mounted; open or closed system. Gas or water-cooled. Standard or lightweight.
- **MIG** Short-arc. Spray-arc. Dynamic-arc.
- **MANUAL METAL ARC** Standard materials. Special materials.
- **PRIMARY SWITCHED 25K Hz** transistorised power source; very low energy use with savings of up to 35% or more on electricity.
- **POSSIBILITY OF SPATTER-FREE APPLICATIONS** on any material.
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A High Performance Transistorised Power Source for MIG Welding - by A.C.D.R. Rodrigues

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This research concerns an investigation into the application of Power Electronics to high performance power sources for precise and efficient control of the pulsed-current metal-inert gas (PCM) welding processes.

The physical processes of the welding arc are reviewed and the characteristics of a number of power sources are considered prior to preparing the operational specification for the PCM power source. From a number of possibilities the high frequency switching regulator operating in the secondary side of the power transformer was selected for detailed study.

The power source was based on the use of state-of-the-art power transistors operating in a switching mode to minimise losses and to give a fast response for good welding performance. The basic operating frequency was chosen to be at the very limit of the audio range. The dynamic behaviour of the transistors and associated protection networks is critical and failure to meet all the operating limits of the transistor can be costly. To assist with the thorough understanding of the circuit behaviour and to predict the transistor switching waveforms a digital computer model was developed. This gave good correlation with experimental results observed with the completed power source.

Tests were carried out with the welding power source and showed that there was no discernable difference in the weld quality when compared with those produced by the more expensive series linear regulator power source. As a direct result of the study a new range of power sources meeting exacting standards have been made available to the welding industry.
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